DDR5 SDRAM U-DIMM
Based on 16Gb M-die

HMCG66MEBUAxxxN
HMCG78MEBUAxxxN
HMCG88MEBUAxxxN
HMCG78MEBEAxxxN
HMCG88MEBEAxxxN

*SK hynix reserves the right to change products or specifications without notice.

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Release	May.2020	
0.2	Modified Part Number	Jul.2020	
0.3	Updated Pin assignment	Nov.2020	
0.4	Added Part Number Decoder	Jan.2021	
1.0	Updated IDD Specification	Mar.2021	

Description

SK hynix Unbuffered DDR5 SDRAM DIMMs (Unbuffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR5 SDRAM devices. These Unbuffered SDRAM DIMMs are intended for use as main memory when installed in systems such as PCs and workstations.

Features

- DRAM VDD/VDDQ = 1.1V (-33mV / +66mV)
- DRAM VPP = 2.5V (–125mV / +250mV)
- 32 Bank with x4/x8
- 16 Bank with x16
- 8 BG(Bank Group) for X4/X8/X16 configurations
- BL16, BC8 OTF, BL32, BL32 OTF supported
- Temperature Encoding
- Same Bank Refresh
- VrefDQ / VrefCA / VrefCS Training
- Hard/Soft Post Package Repair
- Input Clock Frequency Change
- Maximum Power Saving Mode (MPSM)
- Multi-Purpose Command (MPC)
- Per DRAM Addressability (PDA)
- Read Training Mode
- CA Training Mode
- CS Training Mode
- Per Pin VREFDQ Training
- Write Leveling Training Mode
- Connectivity Test (CT)
- ZQ Calibration
- DFE (Decision Feedback Equalization) for DQ
- DQS Interval Oscillator
- 1N / 2N Mode support for Commands
- On-Die ECC
- ECC Transparency and Error Scrub
- CRC (Cyclic Redundancy Check)
- Loopback for multiple purposes - monitor data, BER(Bit Error Rate) analysis, etc.
- Package Output Driver Test Mode
- Training Modes:
    - VrefDQ / VrefCA / VrefCS Training
    - Read Training Mode
    - CA Training Mode
    - CS Training Mode
    - Per Pin VREFDQ Training
    - Write Leveling Training Mode
    - Duty Cycle Adjuster (DCA) for Read - Global
    - Per Pin DCA(Duty Cycle Adjuster) for Read - Per Pin(DQ)

Ordering Information

Part Number	Density	Organization	Component Composition	# of ranks
HMCG66MEBUAxxxN	8GB	1Gx64	1Gx16(H5CG46MEBDXxxx)*4	1
HMCG78MEBUAxxxN	16GB	2Gx64	2Gx8(H5CG48MEBDXxxx)*8	1
HMCG88MEBUAxxxN	32GB	4Gx64	2Gx8(H5CG48MEBDXxxx)*16	2
HMCG78MEBEAxxxN	16GB	2Gx72	2Gx8(H5CG48MEBDXxxx)*10	1
HMCG88MEBEAxxxN	32GB	4Gx72	2Gx8(H5CG48MEBDXxxx)*20	2

Key Parameters

MT/s	Grade	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR5-4800	-EB	0.416	16.00	16.00	16.00	32.00	48.00	40-39-39

Address Table

		8GB (1Rx16)	16GB (1Rx8)	32GB (2Rx8)
Bank Address	**# of Bank Groups**	4 / 4 / 16	8 / 4 / 32	8 / 4 / 32
	BG Address	BG0~BG1	BG0~BG2	BG0~BG2
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C9	C0~C9	C0~C9
Page size		2KB	1KB	1KB

DDR5 SDRAM DIMM Part Number Decoder

HMX XX X X XX X X XXX X

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

1-3) Product Mode & Type

HMC	DDR5 Module

4-5) Product Density

G6	8GB
G7	16GB
G8	32GB

6) Organization

4	X4
8	X8
6	X16

7) Generation.

M	1st

8-9) Speed

EB	4800 40-39-39

10) Module Type

U	UDIMM	S	SODIMM
E	ECC UDIMM	A	ECC SODIMM

11) Extra Info. (Die density, DIMM Profile, Temperatue)

A	16Gb, Low Profile, CT(0~95°C)

12-14) Serial Code

Code	RCD	DB	PMIC	Etc.
081	-	-	Renesas(IDT) 5100	-
084	-	-	MPS 5100	-
092	-	-	Renesas(IDT) 5100	-
095	-	-	MPS 5100	-

15) Sales Type

N	Normal

※ Codes can be added, deleted or changed by internal management.

※ This decoder can be used only for understanding SK hynix's part number. It doesn't mean supportability for all kinds of products.

Pin Descriptions

Pin Name	Description	Pin Name	Description
CA0_A - CA12_A	Command address input to channel A.	CA0_B - CA12_B	Command address input to channel B.
CS0_A_n - CS1_A_n	DIMM Rank Select Lines input for channel A.	CS0_B_n - CS1_B_n	DIMM Rank Select Lines input for channel B.
DQ0_A - DQ31_A	DIMM memory data bus for channel A.	DQ0_B - DQ31_B	DIMM memory data bus for channel B.
CB0_A - CB3_A	DIMM ECC check bits for channel A. (For ECC UDIMM)	CB0_B - CB3_B	DIMM ECC check bits for channel B. (For ECC UDIMM)
CK0_A_t, CK1_A_t	SDRAM clock for channel A. (positive line of differential pair)	CK0_B_t, CK1_B_t	SDRAM clock for channel B. (positive line of differential pair)
CK0_A_c, CK1_A_c	SDRAM clock for channel A. (negative line of differential pair)	CK0_B_c, CK1_B_c	SDRAM clock for channel B. (negative line of differential pair)
DQS0_A_t - DQS4_A_t	Data Buffer data strobes in channel A.(positive line of differential pair)	DQS0_B_t - DQS4_B_t	Data Buffer data strobes in channel B.(positive line of differential pair)
DQS0_A_c - DQS4_A_c	Data Buffer data strobes in channel A.(negative line of differential pair)	DQS0_B_c - DQS4_B_c	Data Buffer data strobes in channel B.(negative line of differential pair)
DM0_A_n - DM3_A_n	SDRAM input data mask signal for write data of channel A.	DM0_B_n- DM3_B_n	SDRAM input data mask signal for write data of channel B.
VIN_BULK	5 V power input supply pin to the PMIC.	VSS	Power supply return (ground)
PWR_GOOD	Output for Power good indicator from the PMIC. The PMIC ensures this pin high when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. Otherwise PMIC will drive this pin low. The PMIC disables its output regulator when this pin is low	PWR_EN	Power Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator.
HSCL	Side-band bus serial bus clock for SPD-Hub.	RESET_n	Set Register and SDRAMs to a Known State
HSDA	Side-band bus serial data line for SPD-Hub.	ALERT_n	Register ALERT_n output
HSA	Side-band bus Host ID and Hub device type ID selection.	RFU	Reserved for future use

Input/Output Functional Descriptions

Symbol	Type	Function
CK_t, CK_c,	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA6_A, CA0_B - CA6_B	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins mat not be interchanged between devices on the same bus.
PAR_A PAR_B		
CS0_A_n - CS1_A_n, CS0_B_n - CS1_B_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DQ0_A - DQ31_A, DQ0_B - DQ31_B	Input	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB0_A - CB3_A, CB0_B - CB3_B	Input	DIMM ECC check bits
DQS0_A_t - DQS4_A_t DQS0_A_c - DQS4_A_c DQS0_B_t - DQS4_B_t DQS0_B_c - DQS4_B_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DM0_A_n-DM3_A_n, DM0_B_n-DM3_B_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
LBDQ	Output	Loopback Data Output: The Output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0]
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HIZ based on MR36:OP[2:0]
ALERT_n	Input/ Output	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
HSCL	Input	Host SidebandBus bus clock, supplied by the master.

Symbol	Type	Function
HSDA	Input/ Output	Host SidebandBus data, connected from the master to bubs or host bus client devices.
HSA	Input	Host SidebandBus bus device ID address pin; input to a hub or other client device to distinguish between identical devices in the I3C Basic address range.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
PWR_EN	Input	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This pin shall not be left floating. If it is not used, it shall be tied to GND.
PWR_GOOD	Input/ Output	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or configured in the appropriate register or and LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
VIN_BULK	Supply	5V power input supply to the PMIC for analog circuits.
VSS	Supply	Ground

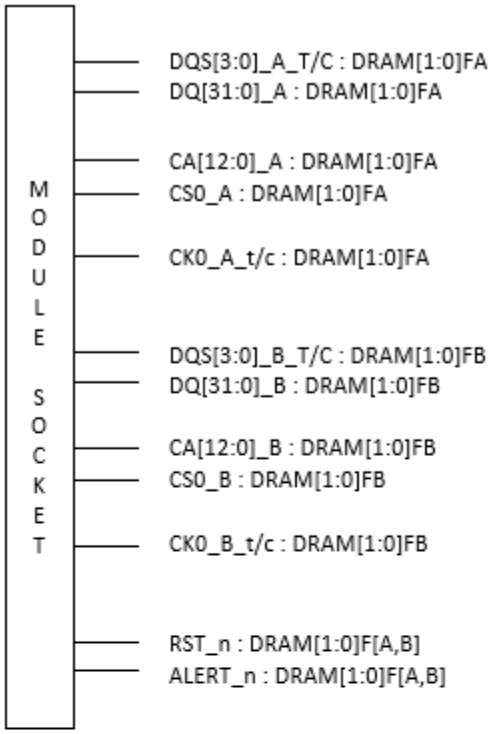
Pin Assignments

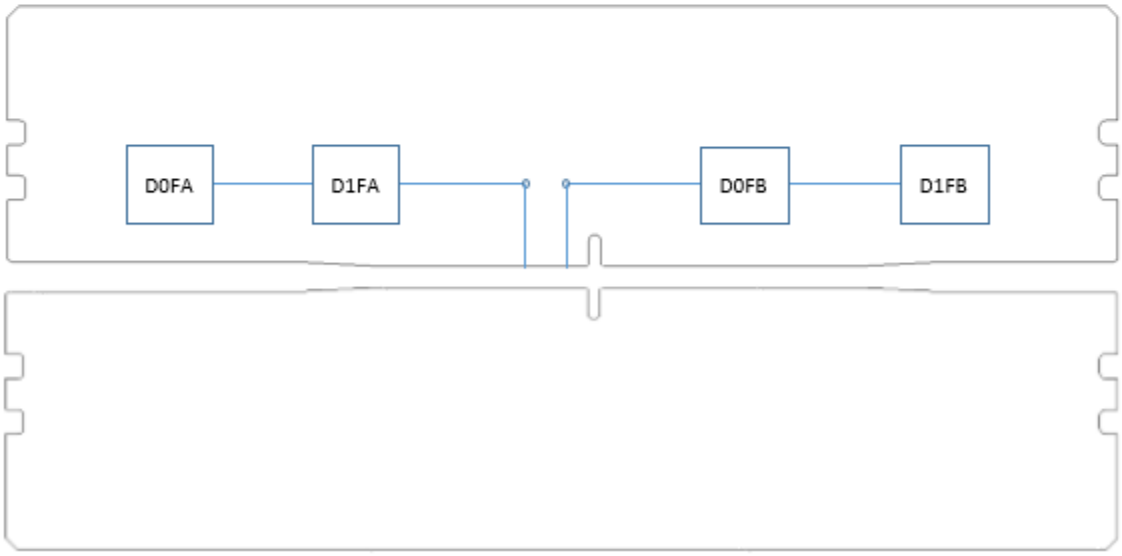
Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
1	VIN_BULK	2	HSA	131	CK0_A_t	132	CK1_A_t
3	VIN_BULK	4	HSCL	133	CK0_A_c	134	CK1_A_c
5	RFU	6	HSDA	135	VSS	136	VSS
7	PWR_GOOD	8	PWR_EN	137	CK0_B_t	138	CK1_B_t
9	VSS	10	VSS	139	CK0_B_c	140	CK1_B_c
11	DQ0_A	12	DQ1_A	141	VSS	142	VSS
13	VSS	14	VSS	143	RFU	144	CA12_B
15	DQ2_A	16	DQ3_A	145	CA11_B	146	CA10_B
17	VSS	18	VSS	147	VSS	148	VSS
19	DM0_A_n	20	DQS0_A_c	149	CA9_B	150	CA8_B
21	VSS	22	DQS0_A_t	151	CA7_B	152	CA6_B
23	DQ4_A	24	VSS	153	VSS	154	VSS
25	VSS	26	DQ5_A	155	CA5_B	156	CA4_B
27	DQ6_A	28	VSS	157	CA3_B	158	CA2_B
29	VSS	30	DQ7_A	159	VSS	160	VSS
31	DQ8_A	32	VSS	161	CS0_B_n	162	CA1_B
33	VSS	34	DQ09_A	163	RESET_n	164	CA0_B
35	DQ10_A	36	VSS	165	CS1_B_N	166	VSS
37	VSS	38	DQ11_A	167	VSS	168	CB0_B
39	DQS1_A_c	40	VSS	169	DQS4_B_c	170	VSS
41	DQS1_A_t	42	DM1_A_n	171	DQS4_B_T	172	CB1_B
43	VSS	44	VSS	173	VSS	174	VSS
45	DQ12_A	46	DQ13_A	175	CB3_B	176	CB2_B
47	VSS	48	VSS	177	VSS	178	VSS
49	DQ14_A	50	DQ15_A	179	DQ0_B	180	DQ1_B
51	VSS	52	VSS	181	VSS	182	VSS
53	DQ16_A	54	DQ17_A	183	DQ2_B	184	DQ3_B
55	VSS	56	VSS	185	VSS	186	VSS
57	DQ18_A	58	DQ19_A	187	DM0_B_n	188	DQS0_B_c
59	VSS	60	VSS	189	VSS	190	DQS0_B_t
61	DM2_A_n	62	DQS2_A_c	191	DQ4_B	192	VSS
63	VSS	64	DQS2_A_t	193	VSS	194	DQ5_B
65	DQ20_A	66	VSS	195	DQ6_B	196	VSS
67	VSS	68	DQ21_A	197	VSS	198	DQ7_B
69	DQ22_A	70	VSS	199	DQ8_B	200	VSS
71	VSS	72	DQ23_A	201	VSS	202	DQ9_B
73	DQ24_A	74	VSS	203	DQ10_B	204	VSS
75	VSS	76	DQ25_A	205	VSS	206	DQ11_B

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
77	DQ26_A	78	VSS	207	DQS1_B_c	208	VSS
79	VSS	80	DQ27_A	209	DQS1_B_t	210	DM1_B_n
81	DQS3_A_c	82	VSS	211	VSS	212	VSS
83	DQS3_A_t	84	DM3_A_n	213	DQ12_B	214	DQ13_B
85	VSS	86	VSS	215	VSS	216	VSS
87	DQ28_A	88	DQ29_A	217	DQ14_B	218	DQ15_B
89	VSS	90	VSS	219	VSS	220	VSS
91	DQ30_A	92	DQ31_A	221	DQ16_B	222	DQ17_B
93	VSS	94	VSS	223	VSS	224	VSS
95	CB0_A	96	CB1_A	225	DQ18_B	226	DQ19_B
97	VSS	98	VSS	227	VSS	228	VSS
99	CB2_A	100	DQS4_A_c	229	DM2_B_n	230	DQS2_B_c
101	VSS	102	DQS4_A_t	231	VSS	232	DQS2_B_t
103	CB3_A	104	VSS	233	DQ20_B	234	VSS
105	VSS	106	CS0_A_n	235	VSS	236	DQ21_B
107	CA0_A	108	ALERT_n	237	DQ22_B	238	VSS
109	CA1_A	110	CS1_A_n	239	VSS	240	DQ23_B
111	VSS	112	VSS	241	DQ24_B	242	VSS
113	CA2_A	114	CA3_A	243	VSS	244	DQ25_B
115	CA4_A	116	CA5_A	245	DQ26_B	246	VSS
117	VSS	118	VSS	247	VSS	248	DQ27_B
119	CA6_A	120	CA7_A	249	DQS3_B_c	250	VSS
121	CA8_A	122	CA9_A	251	DQS3_B_t	252	DM3_B_n
123	VSS	124	VSS	253	VSS	254	VSS
125	CA10_A	126	CA11_A	255	DQ28_B	256	DQ29_B
KEY				257	VSS	258	VSS
127	CA12_A	128	RFU	259	DQ30_B	260	DQ31_B
129	VSS	130	VSS	261	VSS	262	VSS

Block Diagram

8GB, 1Gx64 Module (1Rank of x16) NECC U-DIMM - page1

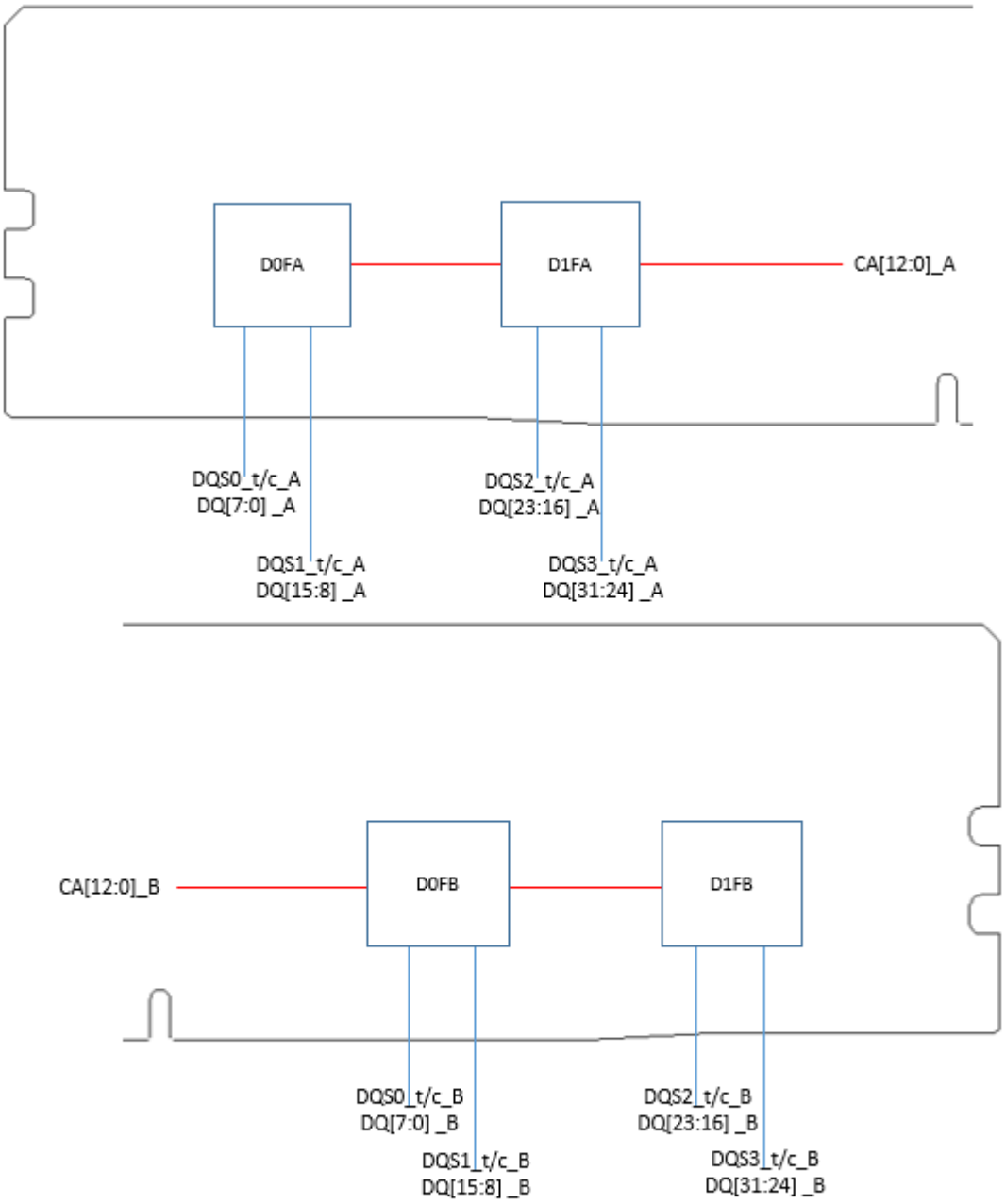




Note :

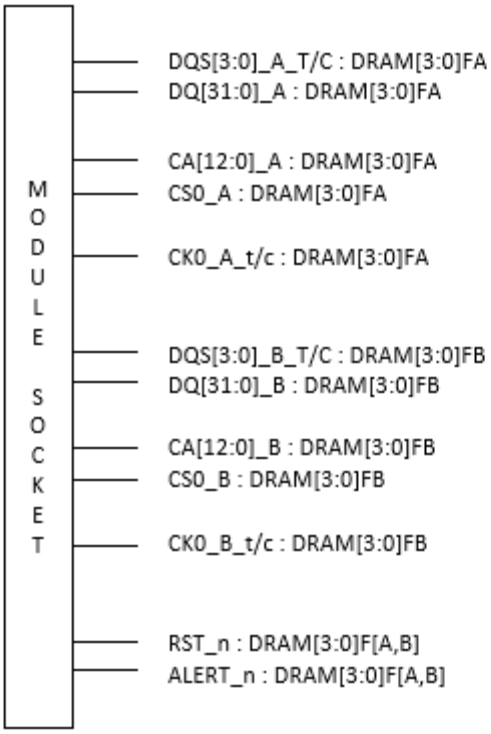
1. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

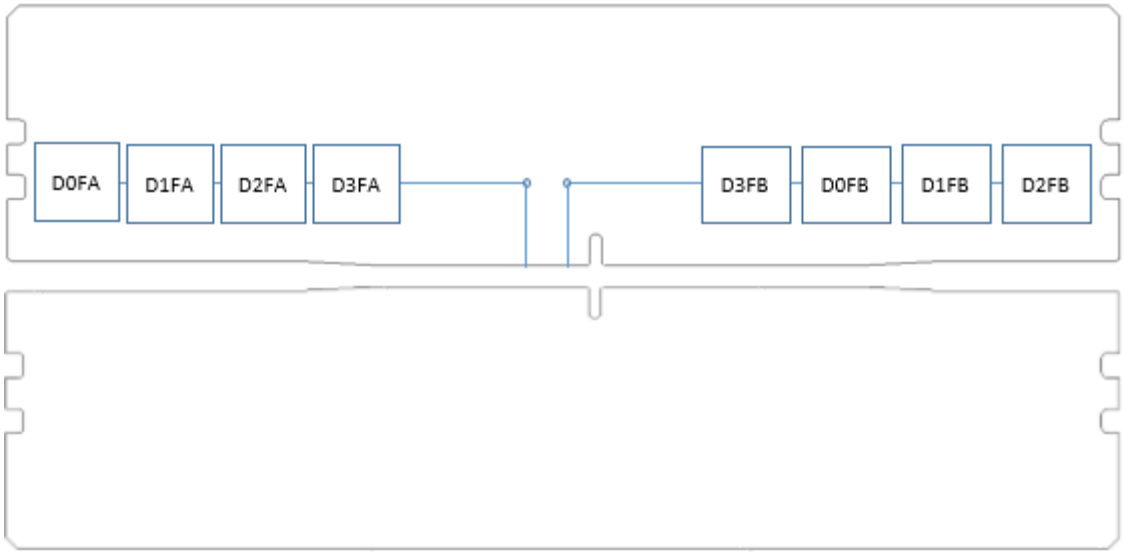
8GB, 1Gx64 Module (1Rank of x16) NECC U-DIMM - page2



Note :
1. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

16GB, 2Gx64 Module (1Rank of x8) NECC U-DIMM - page1

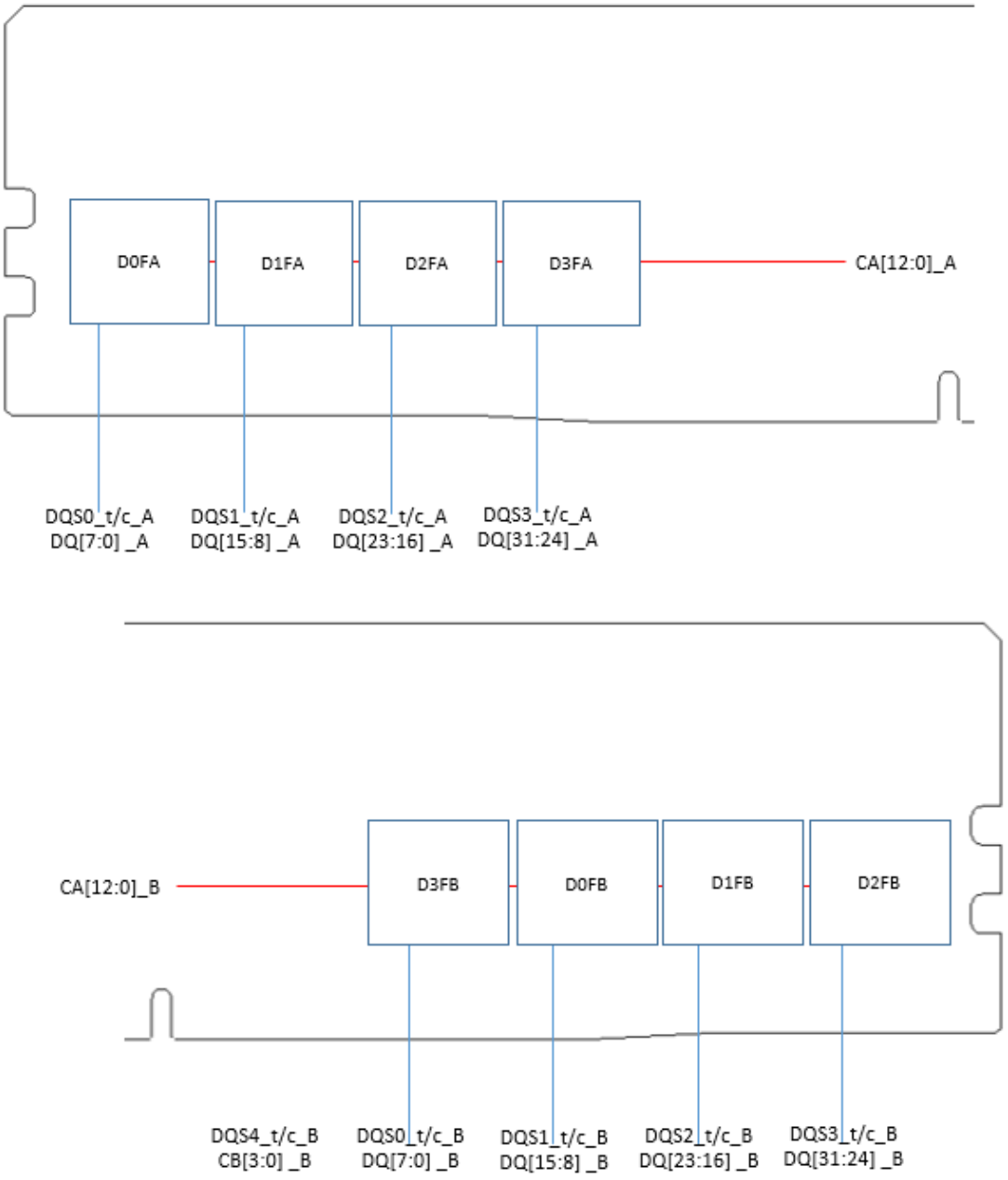




Note :

1. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

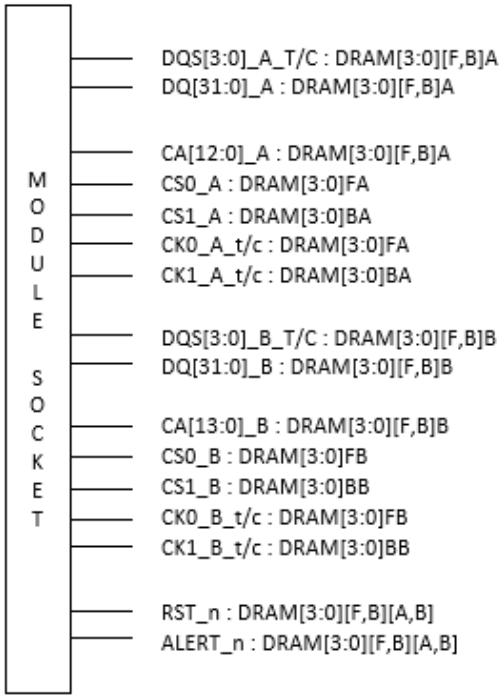
16GB, 2Gx64 Module (1Rank of x8) NECC U-DIMM - page2

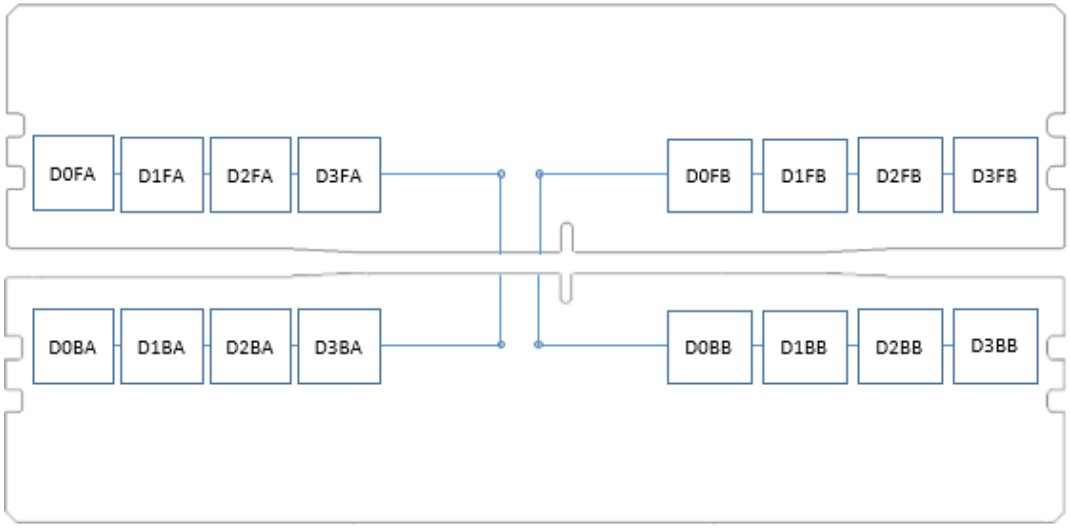


Note :

1. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

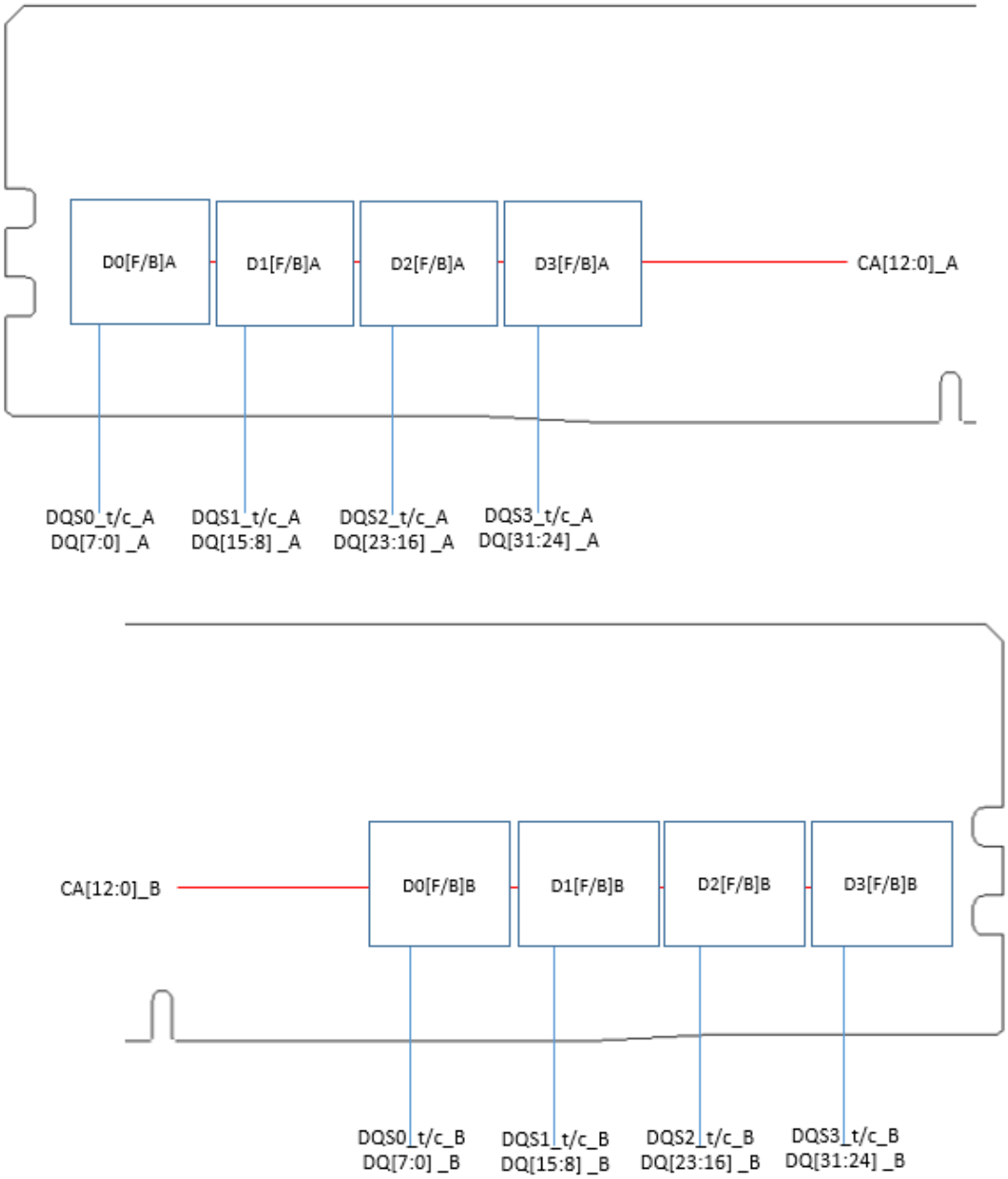
32GB, 4Gx64 Module (2Rank of x8) NECC U-DIMM - page1





Note :
1. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

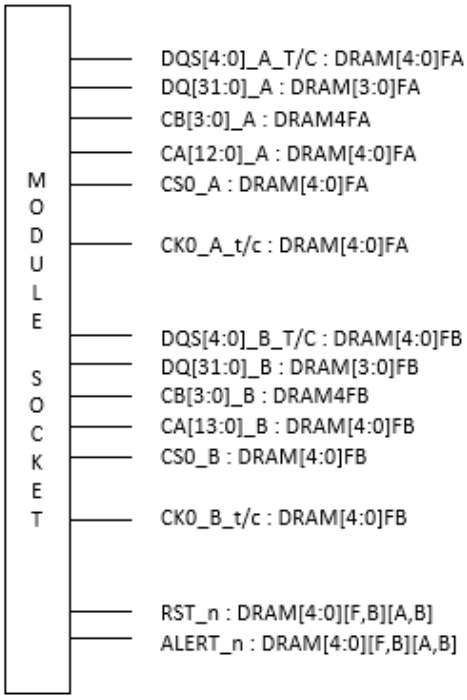
32GB, 4Gx64 Module (2Rank of x8) NECC U-DIMM - page2

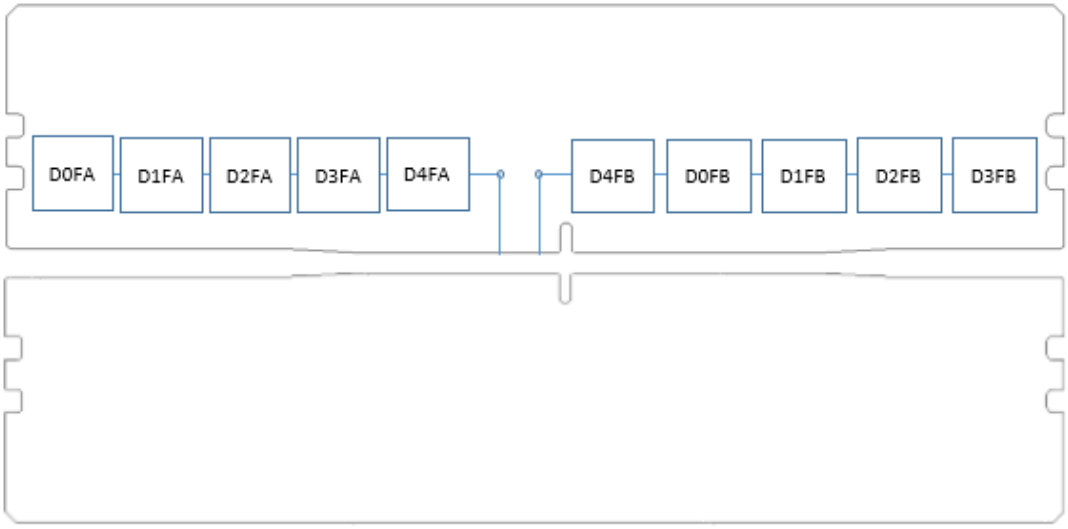


Note :

1. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

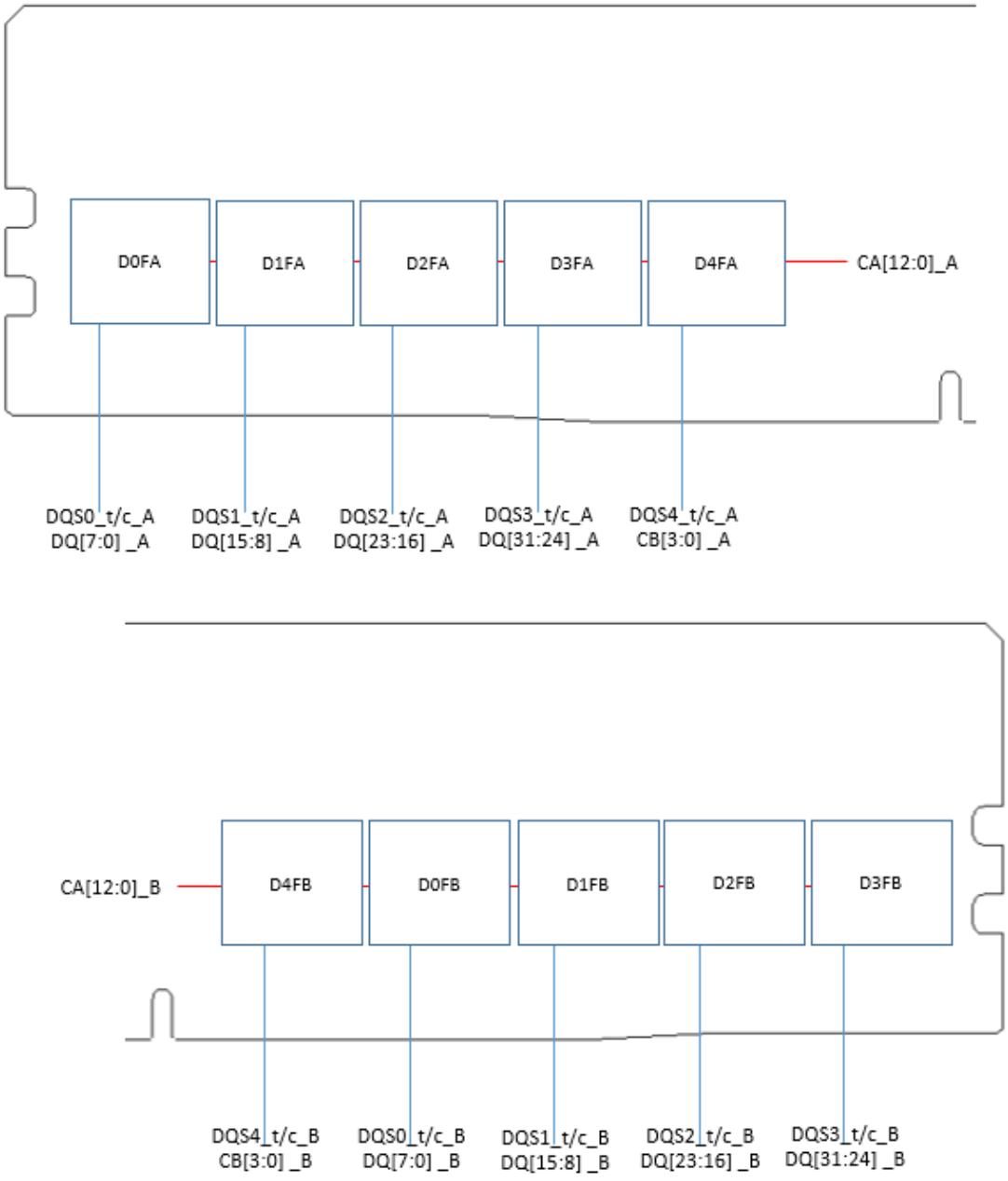
16GB, 2Gx72 Module (1Rank of x8) ECC U-DIMM - page1





Note :
1. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

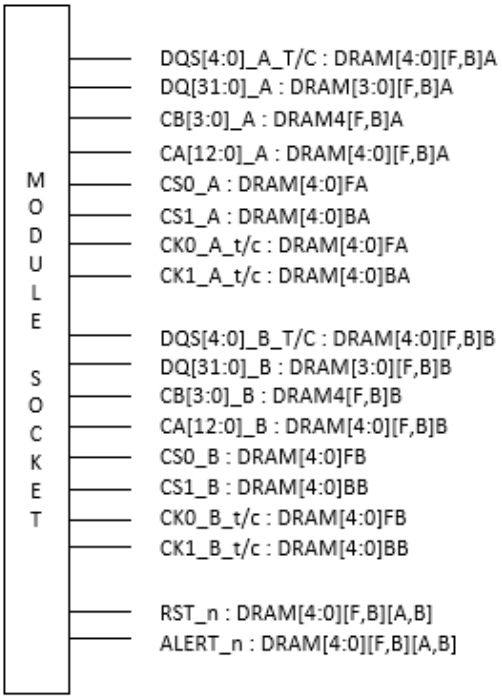
16GB, 2Gx72 Module (1Rank of x8) ECC U-DIMM - page2

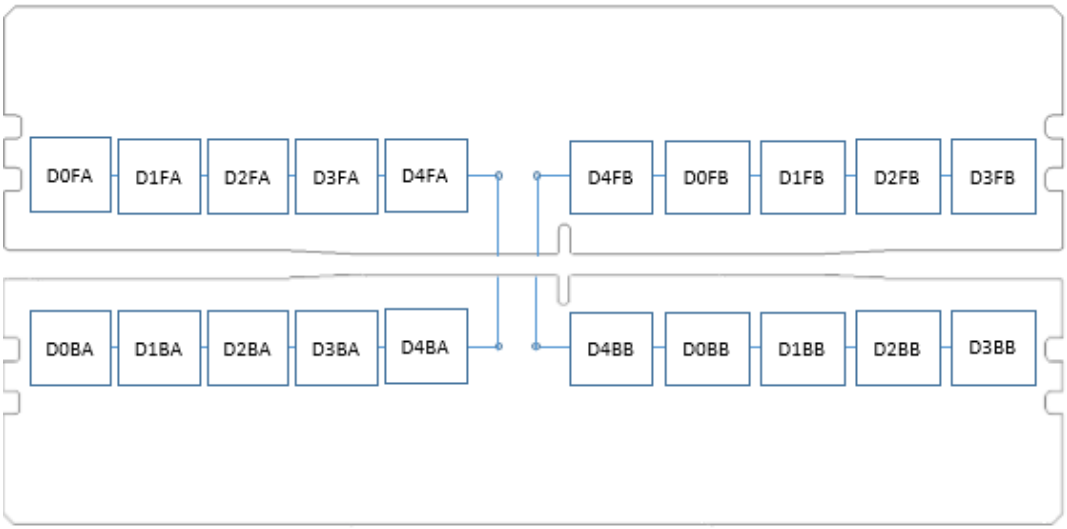


Note :

1. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

32GB, 4Gx72 Module (2Rank of x8) ECC U-DIMM - page1

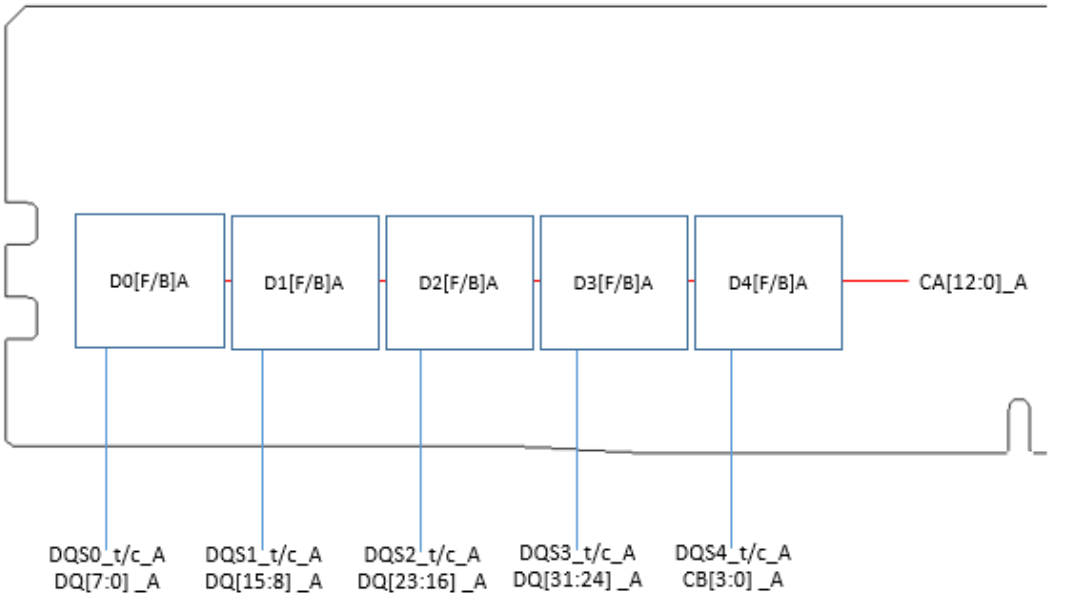


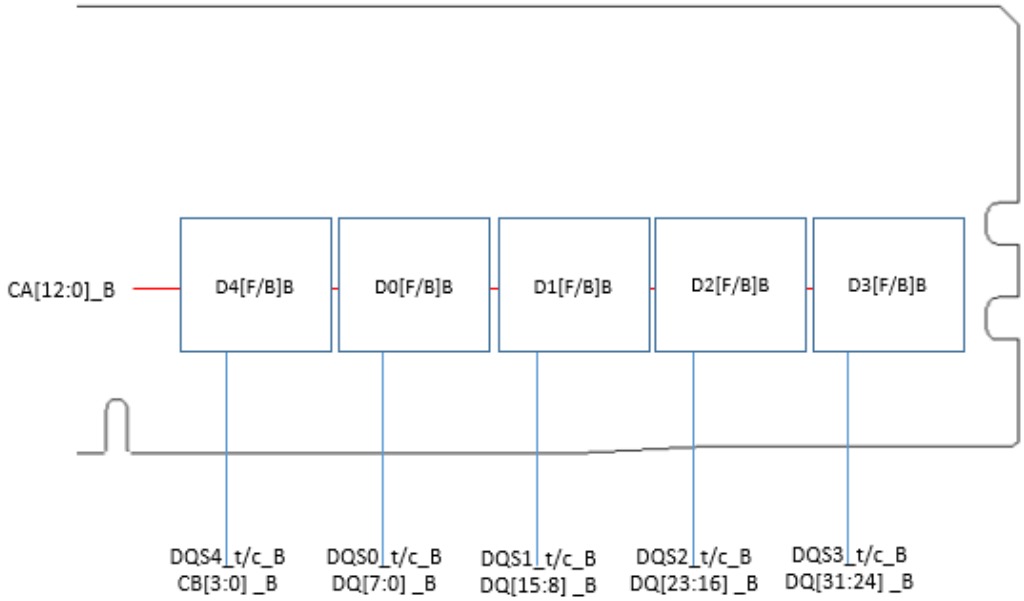


Note :

1. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

32GB, 4Gx72 Module (2Rank of x8) ECC U-DIMM - page2





Note :

1. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 2.1	V	4
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.3 ~ 1.5	V	1,3,5
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Note(s):
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times. When VDD and VDDQ are less than 500 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.
5.Overshoot area above 1.5 V is specified in Section 8.3.4, Section 8.3.5, and Section 8.3.6.

tREFI parameters for REFab and REFsb Commands

Command	Refresh Mode	Symbol & Reange		Expression	Value	Unit	Notes
REFab	Normal	tREFI1	0°C <= TCASE <= 85°C	rREFI	3.9	us.	
			85°C < TCASE<= 95°C	rREFI/2	1.95	us.	
REFab	Fine Granularity	tREFI2	0°C <= TCASE <= 85°C	rREFI/2	1.95	us.	
			85°C < TCASE<= 95°C	rREFI/4	0.975	us.	
REFsb	Fine Granularity	tREFIsb	0°C <= TCASE <= 85°C	rREFI/(2*n)	1.95/n	us.	1
			85°C < TCASE<= 95°C	rREFI/(4*n)	0.975/n	us.	1

Note(s):

1. n is the number of banks in a bank group (eg. 8G: n=2; 16G: n=4)

AC & DC Operating Conditions

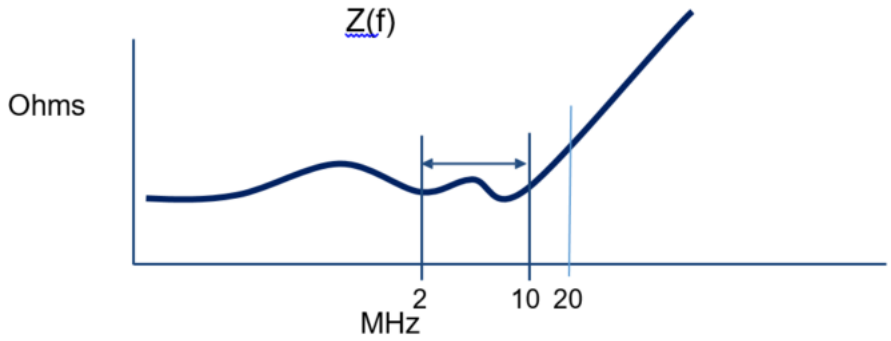
Recommended DC Operating Conditions

Symbol	Parameter	Low Freq Voltage Spec Freq: DC to 2MHz				Z(f) Spec Freq: 2Mhz to 10Mhz		Z(f) Spec Freq: 20Mhz		Notes
		Min.	Typ.	Max.	Unit	Zmax	Unit	Zmax	Unit	
VDD	Device Supply Voltage	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm	1,2,3
VDDQ	Supply Voltage for I/O	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm	1,2,3
VPP	Core Power Voltage	1.746 (-3%)	1.8	1.908 (+6%)	V	10	mOhm	20	mOhm	3

Note(s):

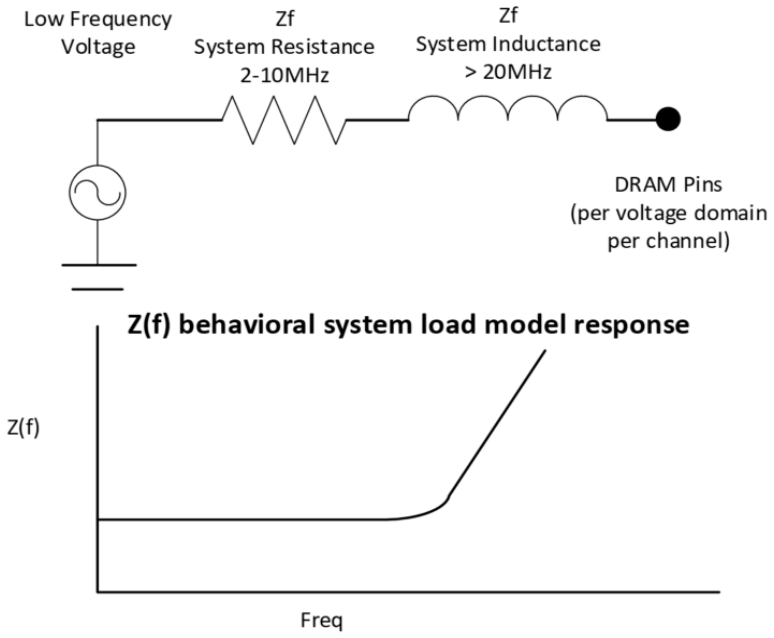
1. VDD must be within 66mv of VDDQ
2. AC parameters are measured with VDD and VDDQ tied together.
3. This includes all voltage noise from DC to 2 MHz at the DRAM package ball.
4. Z(f) is defined for all pins per voltage domain. Z(f) does not include the DRAM package and silicon die.

Zprofile/Z(f) of the system at the DRAM package solder ball (without DRAM component)



Zprofile/Z(f) of the system at the DRAM package solder ball (without DRAM component)

A simplified electrical system load model for Z(F) with the general frequency response is shown in the figure below. The resistance and inductance can be scaled to generalize the spec response to the DRAM pin.



Simplified Z(f) electrical model and frequency response of PDN at the DRAM pin without the DRAM component

1. AC & DC Input Measurement Levels

1.1 Overshoot and Undershoot specifications for CAC - No Ballot

1.2 CA Rx voltage and timings

Note: The following draft assumes internal CA VREF. If the VREF is external, the specs will be modified accordingly.

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

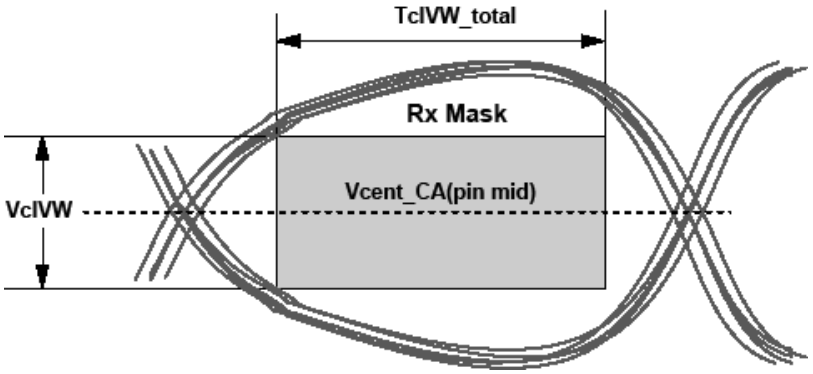


Figure 1 — CA Receiver (Rx) mask

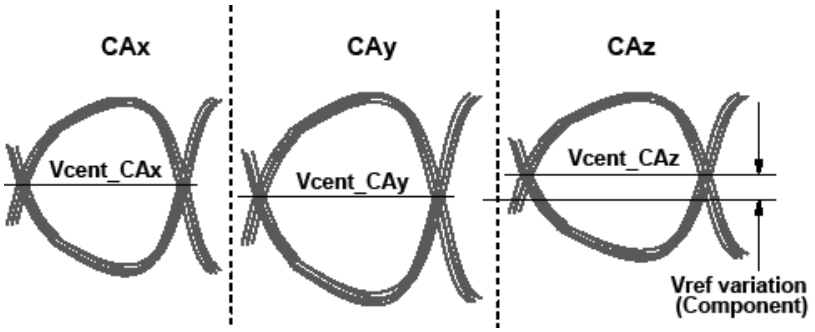
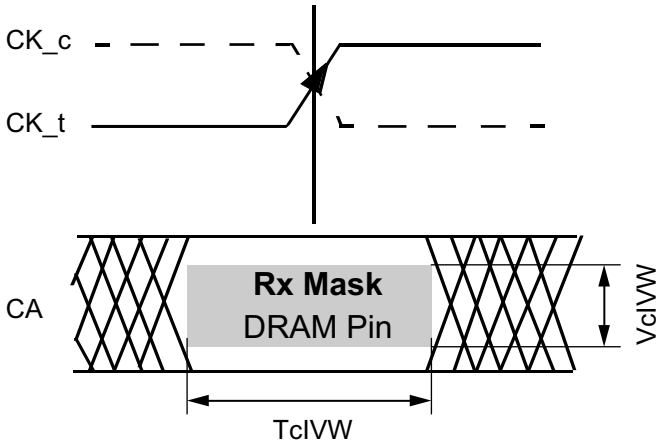


Figure 2 — Across pin V_{REF}CA voltage variation

Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 3. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level V_{REF} will be set by the system to account for Ron and ODT settings.

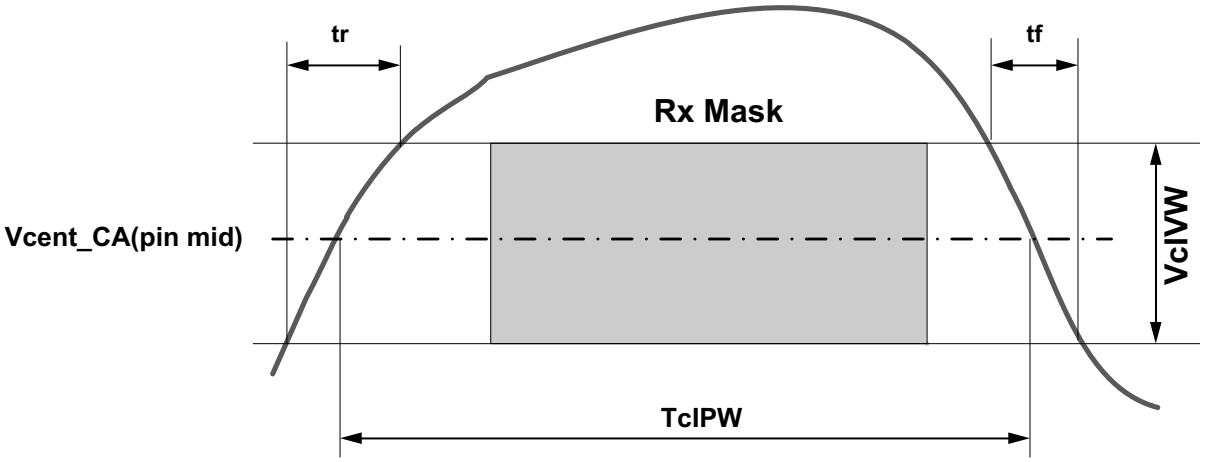
CK_t, CK_c, CA Eye at DRAM Pin

Optimally centered Rx mask



TcIVW is not necessarily center aligned on CK_t/CK_c crossing at the DRAM pin, but is assumed to be center aligned at the DRAM Latch.

Figure 3 — CA Timings at the DRAM Pins



Note
1. SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 4 — CA TcIPW and SRIN_cIVW definition (for each input pulse)

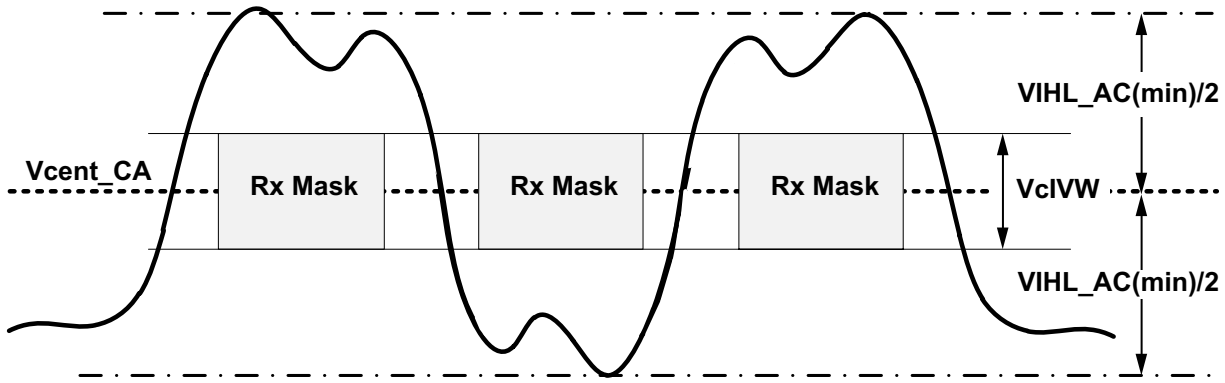


Figure 5 — CA VIHL_AC definition (for each input pulse)

Table 1 — DRAM CA, CS Parametric values for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	-	140	-	140	-	140	-	130	-	130	mV	1,2,4
Rx Timing Window	TcIVW	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	UI*	1,2,3,4, 8
CA Input Pulse Amplitude	VIHL_AC	160		160		160		150		150		mV	7
CA Input Pulse Width	TcIPW	0.58		0.58		0.58		0.58		0.58		UI*	5,8
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	1	7	1	7	1	7	V/ns	6

Note(s):

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
7. VIHL_AC does not have to be met when no transitions are occurring.
8. *** UI=tCK(avg)min**

1.3 Input Clock Jitter Specification

1.3.1 Overview

The clock is being driven to the DRAM either by the RCD for L/RDIMM modules, or by the host for U/SODIMM modules (**Figure 6**).

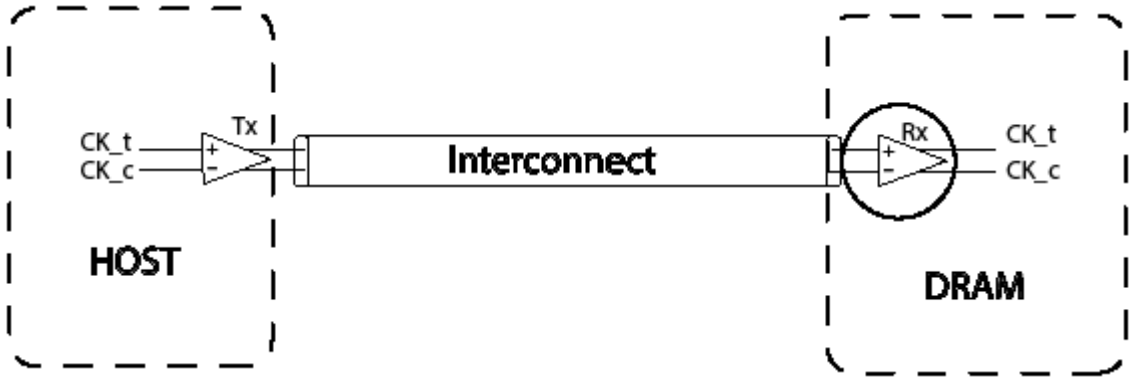


Figure 6 — HOST driving clock signals to the DRAM

1.3.2 Specification for DRAM Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5 SDRAM device.

Table 2 — DRAM Input Clock Jitter Specifications for DDR5-3200 to 4400

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DRAM Reference clock frequency	tCK	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	MHz	1,11
Duty Cycle Error	tCK_Duty_UI_Error	-	0.05	-	0.05	-	0.05	-	0.05		0.05	UI	1,4,11
Rj RMS value of 1-UI Jitter	tCK_1UI_Rj_NoBUJ	-	0.0037	-	0.0037	-	0.0037	-	0.0037	-	0.0037	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	tCK_1UI_Dj_NoBUJ	-	0.030	-	0.030	-	0.030	-	0.030	-	0.030	UI	3,6,11
Tj value of 1-UI Jitter	tCK_1UI_Tj_NoBUJ	-	0.090	-	0.090	-	0.090	-	0.090	-	0.090	UI	3,6,11
Rj RMS value of N-UI Jitter, where N=2,3	tCK_NUI_Rj_NoBUJ, where N=2,3	-	0.0040	-	0.0040	-	0.0040	-	0.0040	-	0.0040	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N=2,3	tCK_NUI_Dj_NoBUJ, where N=2,3	-	0.074	-	0.074	-	0.074	-	0.074	-	0.074	UI	3,7,11
Tj value of N-UI Jitter, where N=2,3	tCK_NUI_Tj_NoBUJ, where N=2,3	-	0.140	-	0.140	-	0.140	-	0.140	-	0.140	UI	3,8,11
Rj RMS value of N-UI Jitter, where N=4,5,6,...,30	tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	UI	3,10,11,12
Tj value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	UI	3,10,11,12

Note(s):

1. f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0=1600
2. Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock
3. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11. The validation methodology for these parameters will be covered in future ballots
12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

1.4 Differential Input Clock (CK_t, CK_c) Cross Point Voltage (VIX)

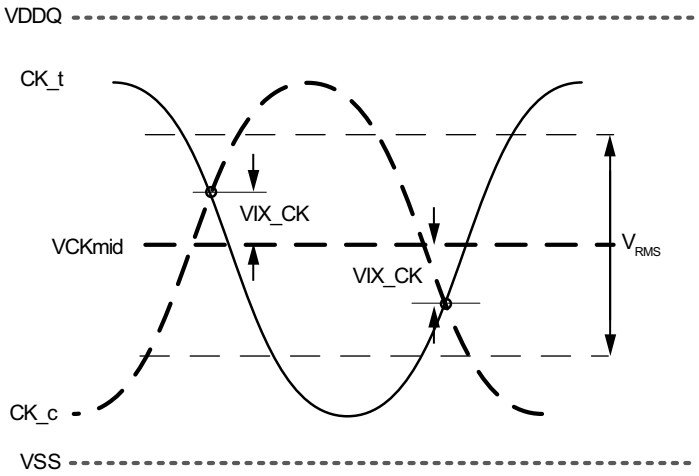


Figure 139 - VIX Definition (CK)

Table 3 — Crosspoint Voltage (VIX) for Differential Input Clock

Parameter	Symbol	DDR5-3200 - 4800				Unit	Notes
		Min	Max				
Clock differential input crosspoint voltage ratio	VIX_CK_Ratio	-	50	-	TBD	%	1,2,3

Note(s):
1. The VIX_CK voltage is referenced to VCKmid(mean) = (CK_t voltage + CK_c voltage) /2, where the mean is over 8 UI
2. VIX_CK_Ratio = (|VIX_CK| / $|V_{RMS}|$)*100%, where V_{RMS} = RMS(CK_t voltage - CK_c voltage)
3. Only applies when both CK_t and CK_c are transitioning

1.5 Differential Input Clock Voltage Sensitivity

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock by varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise. This specifies the Rx voltage sensitivity requirement. The system input swing to the DRAM must be larger than the DRAM Rx at the specified BER

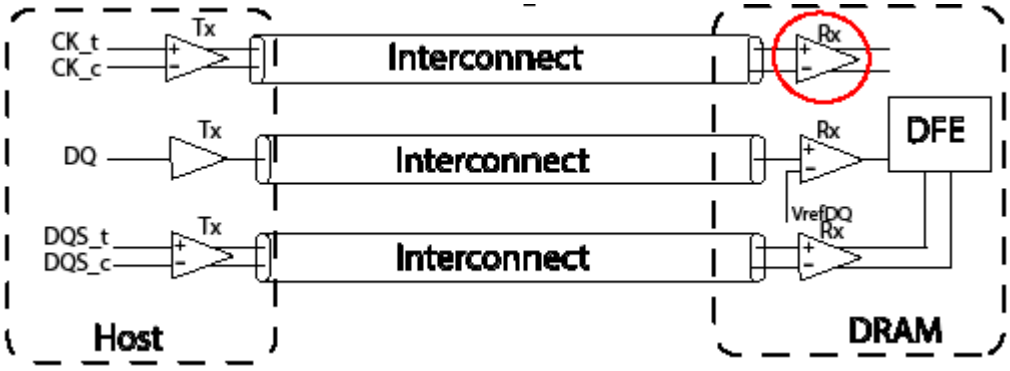


Figure 7 — Example of DDR5 Memory Interconnect

1.5.1 Differential Input Clock Voltage Sensitivity Parameter

Differential input clock (CK_t, CK_c) VRx_CK is defined and measured as shown below. The clock receiver must pass the minimum BER requirements for DDR5.

Table 4 — Differential Input Clock Voltage Sensitivity Parameter for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input Clock Voltage Sensitivity (differential pp)	VRx_CK	-	200	-	200	-	180	-	180	-	160	mV	1,2

NOTE(S):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)

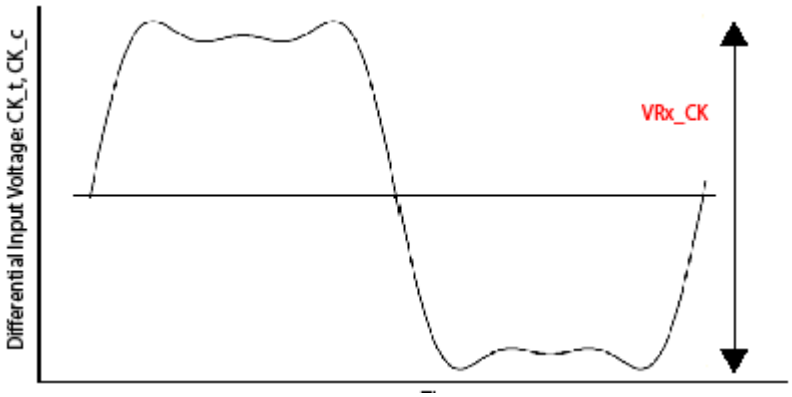


Figure 8 — VRx_CK

1.5.2 Differential Input Voltage Levels for Clock

Table 5 — Differential Clock (CK_t, CK_c) Input Levels for DDR5-3200 to DDR5-6400

From	Parameter	DDR5 3200-6400	Note
$V_{IHdiff}CK$	Differential input high measurement level (CK_t, CK_c)	0.75 x $V_{diffpk-pk}$	1,2
$V_{ILdiff}CK$	Differential input low measurement level (CK_t, CK_c)	0.25 x $V_{diffpk-pk}$	1,2

Note(s):
1. $V_{diffpk-pk}$ defined in **Figure 188**
2. Vdiffpk-pk is the mean high voltage minus the mean low voltage over TBD samples
3. All parameters are defined over the entire clock common mode range

1.5.3 Differential Input Slew Rate Definition for Clock (CK_t, CK_c)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown below.

Figure 9 — Differential Input Slew Rate Definition for CK_t, CK_c

Table 6 — Differential Input Slew Rate Definition for CK_t, CK_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (CK_t - CK_c)	$VIL_{diff}CK$	$VIH_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) / deltaTRdiff	
Differential Input slew rate for falling edge (CK_t - CK_c)	$VIH_{diff}CK$	$VIL_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) / deltaTFdiff	

Note(s):

Table 7 — Differential Input Slew Rate for CK_t, CK_c for DDR5-3200 to DDR5-4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for CK_t, CK_c	SRIdiff_CK	2	14	2	14	2	14	2	14	2	14	V/ns	

Note(s):

1.6 Rx DQS Jitter Sensitivity

The receiver DQS jitter sensitivity test provides the methodology for testing the receiver's strobe sensitivity to an applied duty cycle distortion (DCD) and/or random jitter (Rj) at the forwarded strobe input without adding jitter, noise and ISI to the data. The receiver must pass the appropriate BER rate when no cross-talk nor ISI is applied, and must pass through the combination of applied DCD and Rj.

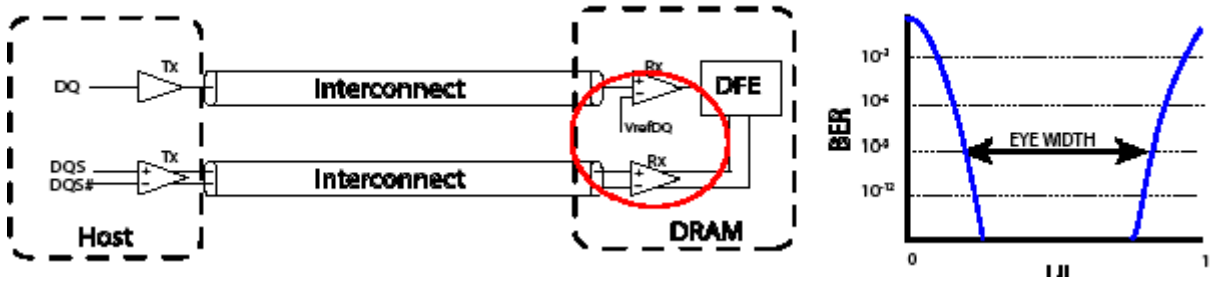


Figure 10 — SDRAM's Rx Forwarded Strobes for Jitter Sensitivity Testing

1.6.1 Rx DQS Jitter Sensitivity Specification

The following table provides Rx DQS Jitter Sensitivity Specification for the DDR5 DRAM receivers when operating at various possible transfer rates. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

Table 8 — Rx DQS Jitter Sensitivity Specification for DDR5-3200 to 4800

[BER = Bit Error Rate; DCD = Duty Cycle Distortion; Rj =Random Jitter]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQ Timing Width	tRx_DQ_tMargin	0.900	-	0.875	-	0.825	-	0.825	-	0.825	-	UI	1,2,3,8, 9,10
Degradation of timing width compared to tRx_DQ_tMargin, with DCD injection in DQS	ΔtRx_DQ_tMargin_ DQS_DCD	-	0.06	-	0.06	-	0.06	-	0.06	-	0.06	UI	1,4,8,9, 10
Degradation of timing width compared to tRx_DQ _tMargin, with Rj injection in DQS	ΔtRx_DQ_tMargin_ DQS_Rj	-	0.09	-	0.09	-	0.09	-	0.09	-	0.09	UI	1,5,8,9, 10
Degradation of timing width compared to tRx_DQ_tMargin, with both DCD and Rj injection in DQS	ΔtRx_DQ_tMargin_ DQS_DCD_Rj	-	0.15	-	0.15	-	0.15	-	0.15	-	0.15	UI	1,2,6,8, 9,10
Delay of any data lane relative to the DQS_t/DQS_c crossing	tRx_DQS2DQ	1	3	1	3	1	3	1	3.25	1	3.5	UI	1,7,8,9, 10

Note(s):

1. Validation methodology will be defined in future ballots. 2UI is defined as 1tCK for this parameter
2. Each of ΔtRx_DQ_tMargin_DQS_DCD, ΔtRx_DQ_tMargin_DQS_Rj, and ΔtRx_DQ_tMargin_DQS _DCD_Rj can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by 5% or more
3. DQ Timing Width - timing width for any data lane using repetitive patterns (check note 4 for the pattern) measured at BER=E-9
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 "1s" and 3 "0s"
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.
6. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.
7. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
8. All measurements at BER=E-9

9. This test should be done after the DQS and DQ Voltage Sensitivity tests are completed and passing

10. The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

1.6.2 Test Conditions for Rx DQS Jitter Sensitivity Tests

Table 2 lists the amount of Duty Cycle Distortion (DCD) and/or Random Jitter (Rj) that must be applied to the forwarded strobe when measuring the Rx DQS Jitter Sensitivity parameters specified in **Table 8** and **Table 194**.

Table 9 — Test Conditions for Rx DQS Jitter Sensitivity Testing for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Applied DCD to the DQS	tRx_DQS_DCD	-	0.045	-	0.045	-	0.045	-	0.045	-	0.045	UI	1,2,3,6, 7,10
Applied Rj RMS to the DQS	tRx_DQS_Rj	-	0.0075	-	0.0075	-	0.0075	-	0.0075	-	0.0075	UI (RMS)	1,2,,4,6, 8,10
Applied DCD and Rj RMS to the DQS	tRx_DQS_DCD_Rj	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	UI	1,2,5,6, 7,9, 10

Note(s):

1. While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
2. The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin
3. Various DCD values should be tested, complying within the maximum limits
4. Various Rj values should be tested, complying within the maximum limits
5. Various combinations of DCD and Rj should be tested, complying within the maximum limits.The maximum timing margin degradation as a result of these injected jitter is specified in a separate table
6. Although DDR5 has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 “1s” and 3 “0s” is used for this test.
7. Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI)
8. RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
9. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
10. The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

1.7 Rx DQS Voltage Sensitivity

1.7.1 Overview

The receiver DQS (strobe) input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

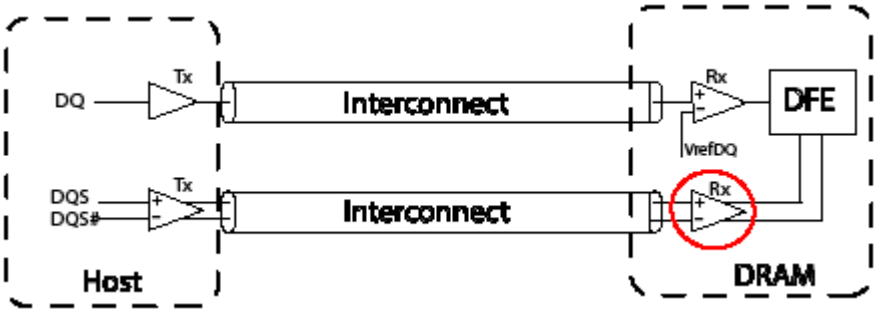


Figure 11 — Example of DDR5 Memory Interconnect

1.7.2 Receiver DQS Voltage Sensitivity Parameter

Input differential (DQS_t, DQS_c) VRx_DQS is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

Table 10 — Rx DQS Input Voltage Sensitivity Parameter for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS Rx Input Voltage Sensitivity (differential pp)	VRx_DQS	-	130	-	115	-	105	-	100	-	100	mV	1,2,3

Note(s):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)
3. Test using clock like pattern of repeating 3 "1s" and 3 "0s"

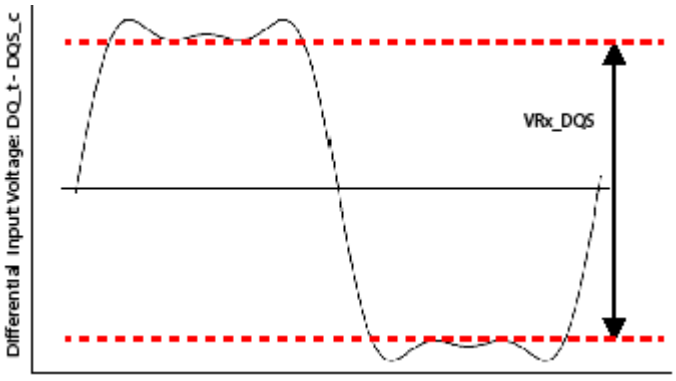


Figure 12 — VRx_DQS

1.8 Differential Strobe (DQS_t, DQS_c) Input Cross Point Voltage (VIX)

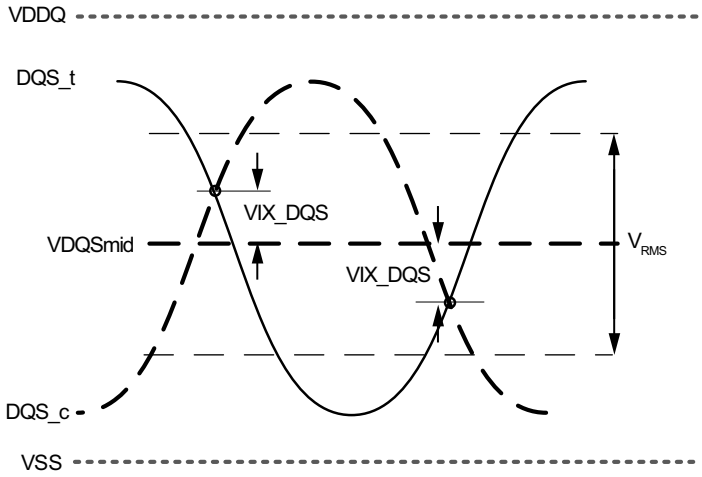


Figure 13 — VIX Definition (DQS)

Table 11 — Crosspoint Voltage (VIX) for DQS Differential Input Signals

Parameter	Symbol	DDR5-3200 - 4800		Unit	Notes
		Min	Max		
DQS differential input crosspoint voltage ratio	VIX_DQS_Ratio	-	50	%	1,2,3

Note(s):
1. The VIX_DQS voltage is referenced to VDQSmid(mean) = (DQS_t voltage + DQS_c voltage) /2, where the mean is over 8 UI
2. VIX_DQS_Ratio = (|VIX_DQS| / |V_{RMS}|)*100%, where V_{RMS} = RMS(DQS_t voltage - DQS_c voltage)
3. Only applies when both DQS_t and DQS_c are transitioning (including preamble)

1.8.1 Differential Input Levels for DQS

Table 12 — Differential Input Levels for DQS (DQS_t, DQS_c) for DDR5-3200 to DDR5-6400

From	Parameter	DDR5 3200-6400	Note
$V_{IHdiff}DQS$	Differential input high measurement level (DQS_t, DQS_c)	0.75 x $V_{diffpk-pk}$	1,2,3
$V_{ILdiff}DQS$	Differential input low measurement level (DQS_t, DQS_c)	0.25 x $V_{diffpk-pk}$	1,2,3

Note(s):
1. $V_{diffpk-pk}$ defined in **Figure 14**
2. $V_{diffpk-pk}$ is the mean high voltage minus the mean low voltage over TBD samples
3. All parameters are defined over the entire clock common mode range

1.8.2 Differential Input Slew Rate for DQS_t, DQS_c

Input slew rate for differential signals are defined and measured as shown below.

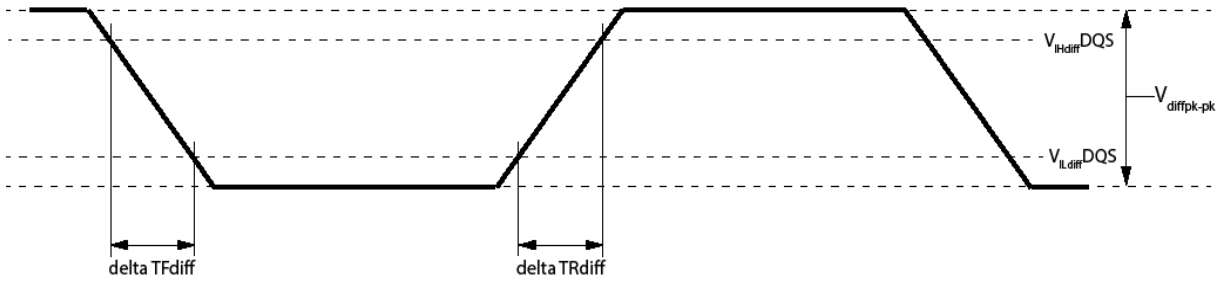


Figure 14 — Differential Input Slew Rate Definition for DQS_t, DQS_c

Table 13 — Differential Input Slew Rate Definition for DQS_t, DQS_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (DQS_t, DQS_c)	$V_{ILdiff}DQS$	$V_{IHdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) /deltaTRdiff	1,2,3
Differential Input slew rate for falling edge (DQS_t, DQS_c)	$V_{IHdiff}DQS$	$V_{ILdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) /deltaTFdiff	1,2,3

Note(s):

Table 14 — Differential Input Slew Rate for DQS_t, DQS_c for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for DQS_t, DQS_c	SRIdiff_DQS	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	V/ns	1

Note(s):

1.9 Rx DQ Voltage Sensitivity

1.9.1 Overview

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

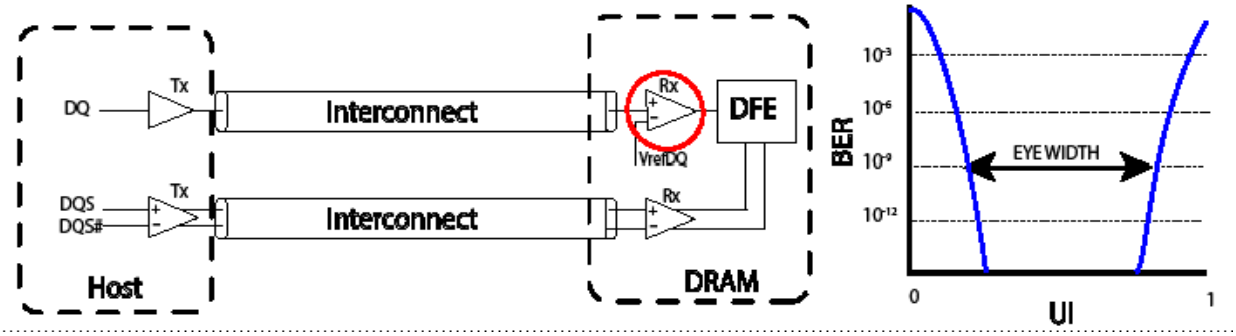


Figure 15 — Example of DDR5 Memory Interconnect

1.9.2 Receiver DQ Input Voltage Sensitivity Parameters

Input single-ended VRx_DQ is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5.

Table 15 — Rx DQ Input Voltage Sensitivity Parameters for DDR5-3200 to 6400

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Minimum DQ Rx input voltage sensitivity applied around Vref	VRx_DQ	-	85	-	75	-	70	-	TBD	mV	1,2

NOTE(S):

1. Refer to the minimum BER requirements for DDR5

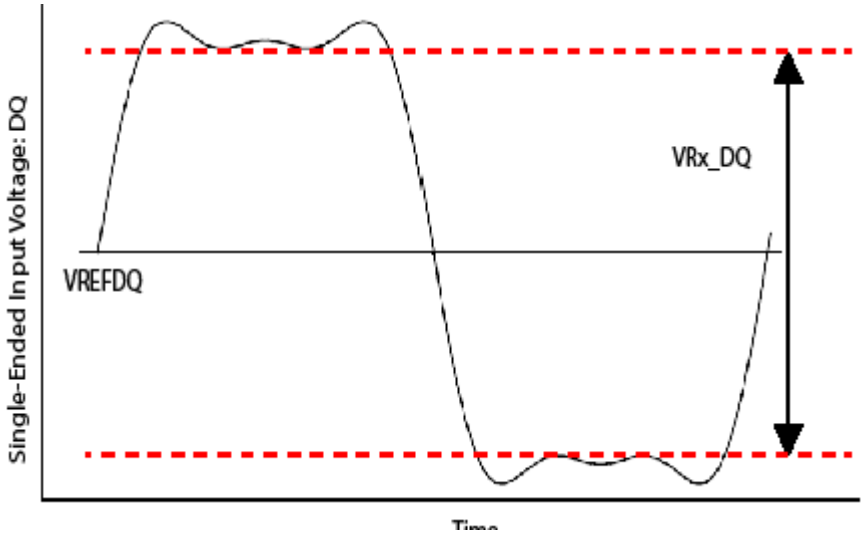
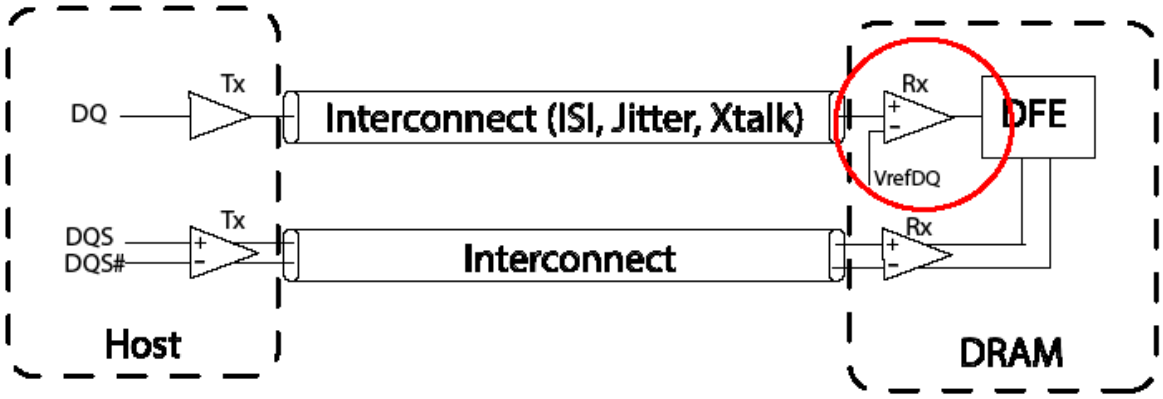


Figure 16 — VRx_DQ

1.10 Rx Stressed Eye

The stressed eye tests provide the methodology for creating the appropriate stress for the DRAM's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.

Figure 17 — Example of Rx Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk



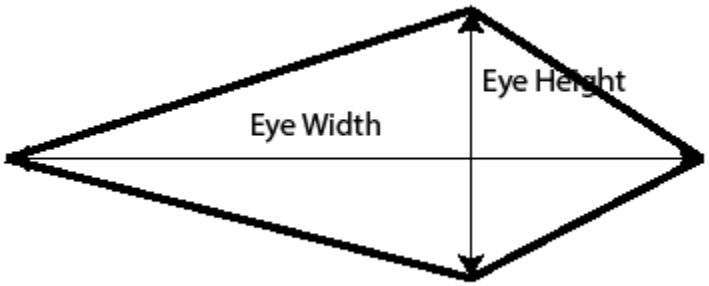


Figure 18 — Example of Rx Stressed Eye Height and Eye Width

1.10.1 Parameters for DDR5 Rx Stressed Eye Tests

Table 16 — Test Conditions for Rx Stressed Eye Tests for DDR5-3200 to 4800

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Eye height of stressed eye for Golden Reference Channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	-	95	-	85	-	80	-	75	-	70	mV	1,2,3,4,5,6,7,8,9
Eye width of stressed eye Golden Reference Channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	UI	1,2,3,4,5,6,7,8,9
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	-	600	-	600	-	600	mV	1.2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	0	0.45	0	0.45	0	0.45	0	0.45	0	0.45	UI p-p	1,2
Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	0	0.04	0	0.04	0	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	0	125	0	125	0	125	mV p-p	1,2
Golden Reference Channel 1 Characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	dB	3

Note(s):

1. Must meet minimum BER of $1E^{-16}$ or better requirement with the stressed eye at the slice of the receiver (after equalization is applied in the summer.) The eye shape is verified by measuring to BER E^{-9} and extrapolating to BER E ^{16}
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 shall be less than 60mV (|Tap-2| + |Tap-3| + |Tap-4| < 60mV).
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth spec, see Recommended DC Operating Conditions
7. The stressed eye is to be assumed to have a diamond shape
8. The VREFDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test, including the limits placed in Note 3
9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location. VrefDQ. and DFE solution to give the best eye margin

1.11 Connectivity Test Mode - Input level and Timing Requirement

During CT Mode, input levels are defined below.

TEN pin: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ

CS_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.

Test Input pins: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.

RESET_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK_t and CK_c signals will be ignored and the DDR5 memory device will enter into the CT mode after time tCT_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on, after RESET_n has de-asserted, the wait time after the RESET_n de-assertion has elapsed, and prior to starting clocks (CK_t, CK_c).

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR5 memory device are unknown and the integrity of the original content of the memory array is not guaranteed; therefore, the reset initialization sequence is required.

All output signals at the test output pins will be stable within tCT_valid after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained High and Low respectively.

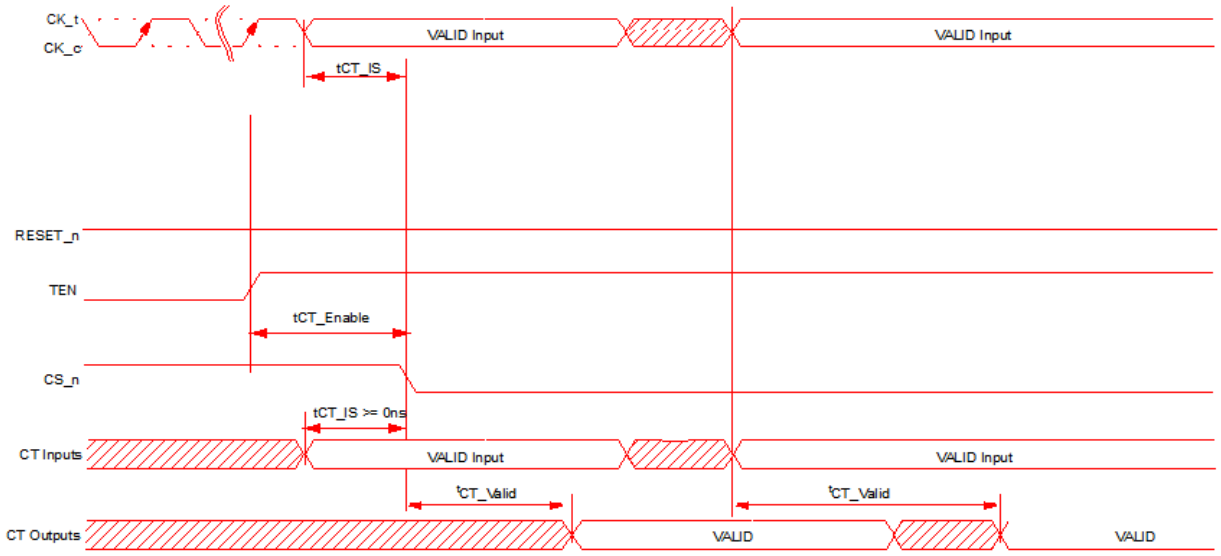


Figure 19 — Timing Diagram for Connectivity Test (CT) Mode

Table 17 — AC parameters for Connectivity Test (CT) Mode

Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_Valid	-	200	ns

1.11.1 Connectivity Test (CT) Mode Input Levels

Following input parameters will be applied for DDR5 SDRAM Input Signals during Connectivity Test Mode.

Table 18 — CMOS rail to rail Input Levels for TEN, CS_n and Test inputs

Parameter	Symbol	Min	Max	Unit	Notes
TEN AC Input High Voltage	VIH(AC)_TEN	0.8 * VDDQ	VDDQ	V	1
TEN DC Input High Voltage	VIH(DC)_TEN	0.7 * VDDQ	VDDQ	V	
TEN DC Input Low Voltage	VIL(DC)_TEN	VSS	0.3 * VDDQ	V	
TEN AC Input Low Voltage	VIL(AC)_TEN	VSS	0.2 * VDDQ	V	2
TEN Input signal Falling time	TF_input_TEN	-	10	ns	
TEN Input signal Rising time	TR_input_TEN	-	10	ns	

Note(s):
1. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
2. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

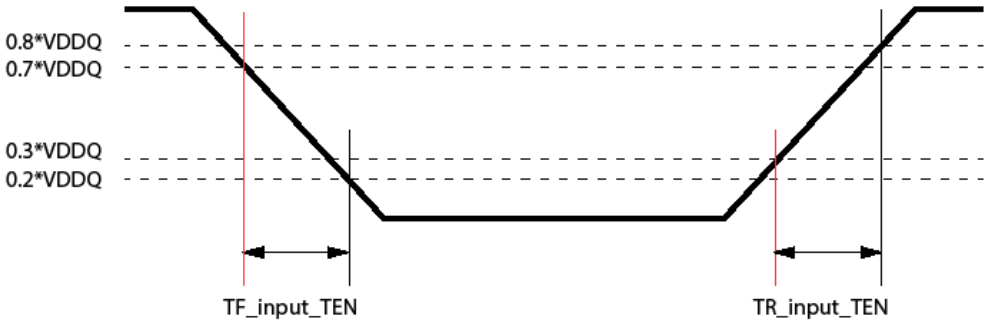


Figure 20 — TEN Input Slew Rate Definition

1.11.2 CMOS rail to rail Input Levels for RESET_n

Table 19 — CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDDQ	VDDQ	V	5
DC Input High Voltage	VIH(DC)_RESET	0.7*VDDQ	VDDQ	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDDQ	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDDQ	V	6
Rising time	TR_RESET	-	1.0	us	
RESET pulse width	tPW_RESET	1.0	-	us	3,4

Note(s):

1.After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. This definition is applied only for “Reset Procedure at Power Stable”.
5. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
6. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

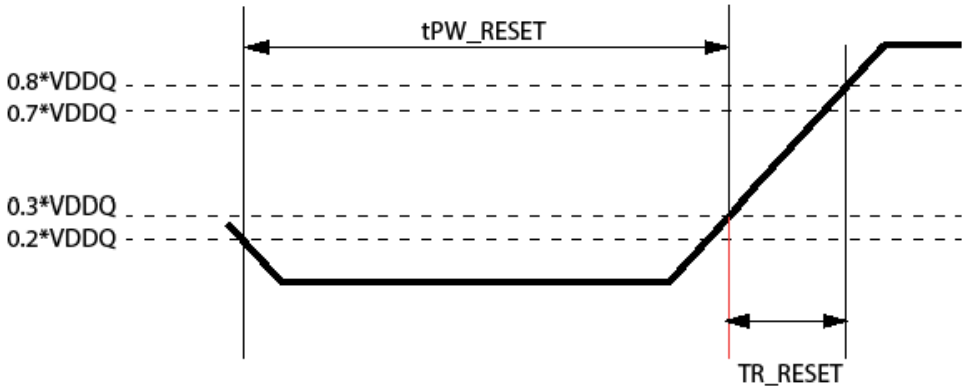


Figure 21 — RESET_n Input Slew Rate Definition

2. AC & DC Output Measurement Levels and Timing

2.1 Output Driver DC Electrical Characteristics for DQS and DQ

The DDR5 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below.

Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

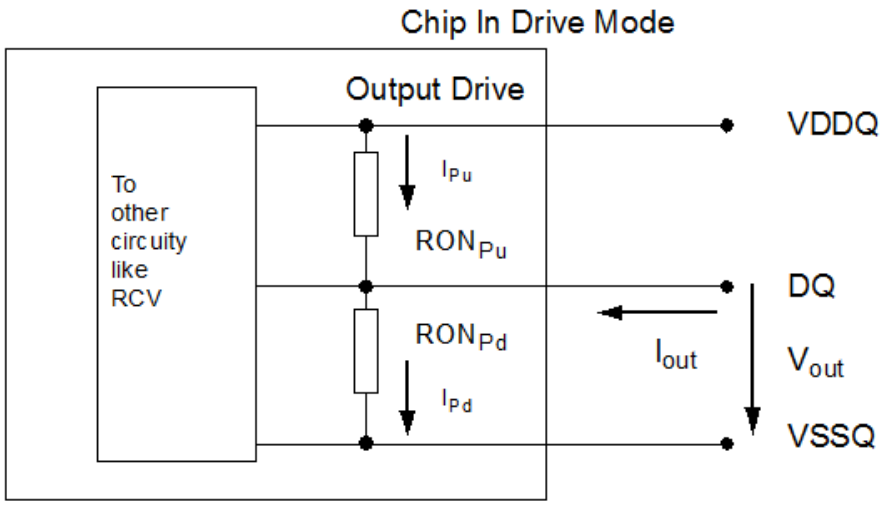


Table 20 — Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE :

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.
3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately;Ron-nom is the nominal Ron value

$$MMPuPd = \frac{RONPu\text{-}RONPd}{RONNOM} * 100$$

4. RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax\text{-}RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax\text{-}RONPdMin}{RONNOM} * 100$$

5. This parameter of x16 device is specified for Upper byte and Lower byte.

2.2 Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ

The DDR5 Loopback driver supports 34 ohms. A functional representation of the output buffer is shown in the figure below.

$$RON_{Pu} = \frac{VDDQ - Vout}{|Iout|}$$ under the condition that RONPd is off

$$RON_{Pd} = \frac{Vout}{|Iout|}$$ under the condition that RONPu is off

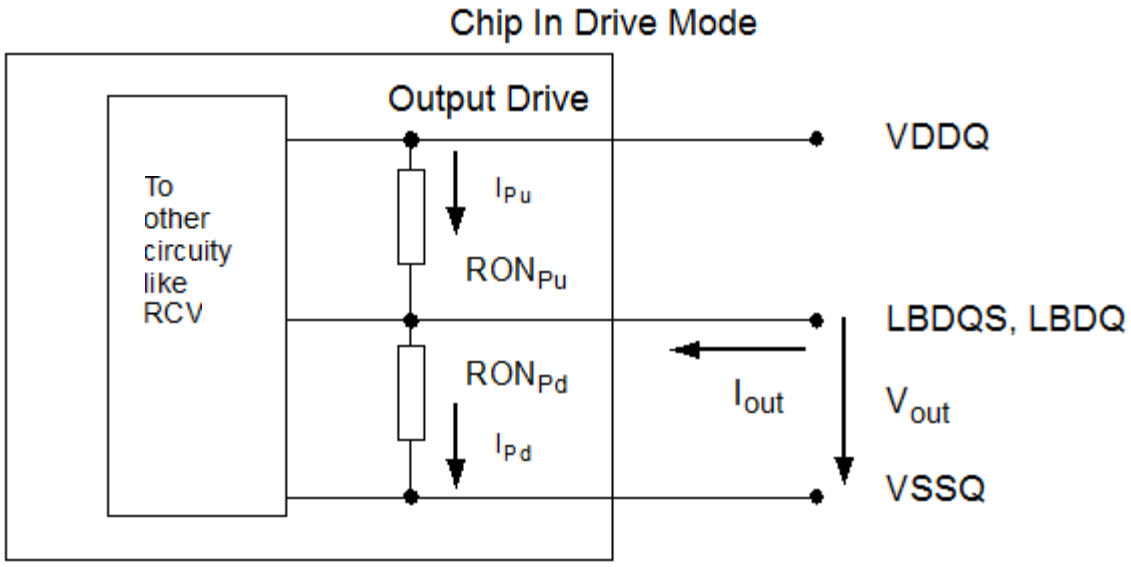


Figure 22 — Output Driver for Loopback Signals

Table 21 — Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch LBDQS-LBDQ within device variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch LBDQS-LBDQ within device variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.

3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately;Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4. RON variance range ratio to RON Nominal value in a given component, including LBDQS and LBDQ.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

2.3 Loopback Output Timing

Loopback strobe LBDQS to Loopback data LBDQ relationship is illustrated in **Figure 23**.

- tLBQSH describes the single-ended LBDQS strobe high pulse width
- tLBQSL describes the single-ended LBDQS strobe low pulse width
- tLBDQSQ describes the latest valid transition of LBDQ measured at both rising and falling edges of LBDQS
- tLBQH describes the earliest invalid transition of LBDQ measured at both rising and falling edges of LBDQS
- tLBDVW describes the data valid window per device per UI and is derived from (tLBQH-tLBDQSQ) of each UI on a given DRAM

Table 22 — Loopback Output Timing Parameters for DDR5-3200 to 4800

Speed		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Loopback Timing													
Loopback LBDQS Output Low Time	tLBQSL	0.7	-	0.7	-	0.7	-	0.7	-	0.7	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	0.7	-	0.7	-	0.7	-	0.7	-	0.7	-	tCK	1
Loopback LBDQS to LBDQ Skew	tLBDQSQ	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK/2	1
Loopback LBDQ Output Time from LB-DQS	tLBQH	3.6	-	3.6	-	3.6	-	3.6	-	3.6	-	tCK/2	1
Loopback Data valid window (tLBQH-tLBDQSQ) of each UI per DRAM	tLBDVW	3.4	-	3.4	-	3.4	-	3.4	-	3.4	-	tCK/2	1

Note(s):

1: Based on Loopback 4-way interleave setting (see MR53)

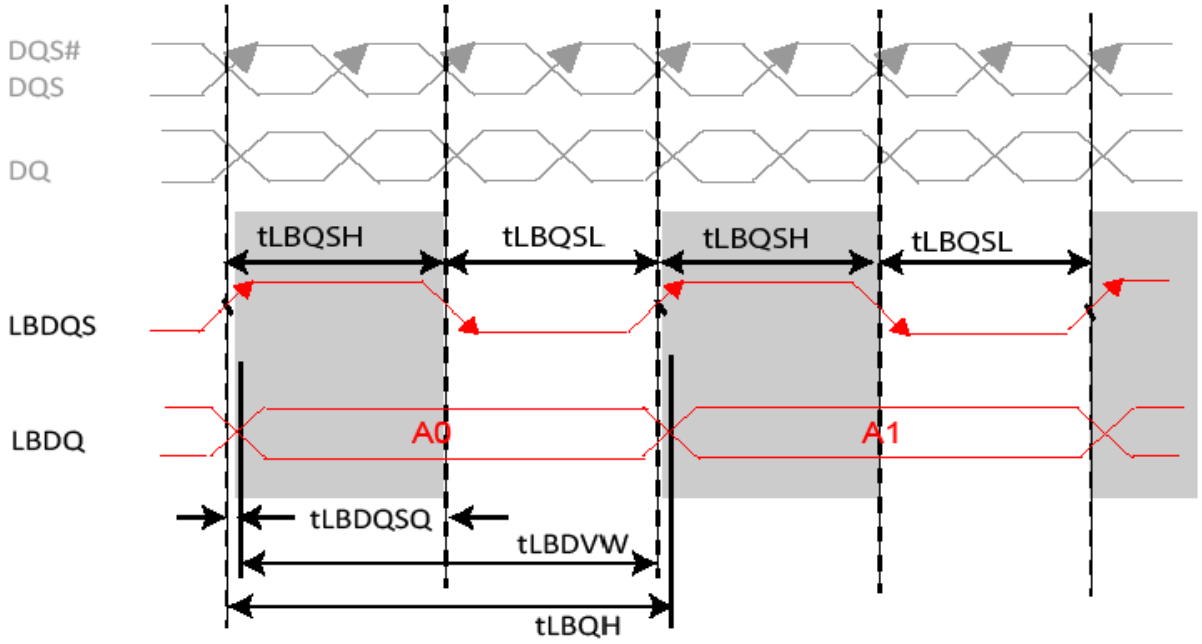
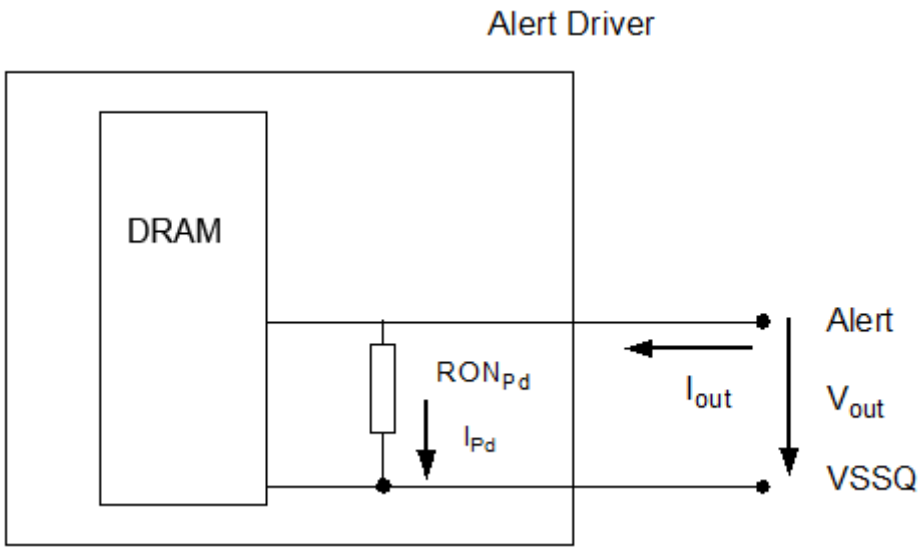


Figure 23 — Loopback Strobe to Data Relationship

2.3.1 Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|Iout|} \quad \text{under the condition that } RON_{Pu} \text{ is off}$$



Resistor	Vout	Min	Max	Unit	NOTE
RON_{Pd}	VOLdc= 0.1* VDDQ	0.3	1.1	$R_{ZQ}/7$	
	V_{OMdc} = 0.8* VDDQ	0.4	1.1	$R_{ZQ}/7$	
	V_{OHdc} = 0.95* VDDQ	0.4	1.25	$R_{ZQ}/7$	

Note(s):

2.3.2 Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied to the Test Output Pin during Connectivity Test (CT) Mode.

The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ}-V_{OUT}}{|Iout|}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|Iout|}$$

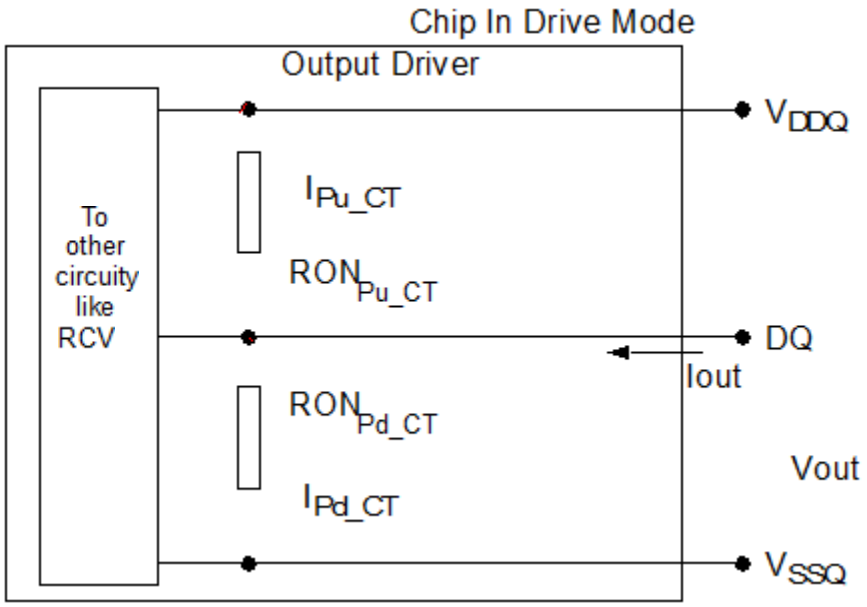


Figure 24 — Output Driver

RONNOM_CT	Resistor	Vout	Max	Units	NOTE
34Ω	RONPd_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2
	RONPu_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2

Note(s):
1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.
2. Uncalibrated drive strength tolerance is specified at +/- 30%

2.4 Single-ended Output Levels - VOL/VOH

Table 23 — Single-ended Output levels for DDR5-3200 to DDR5-6400

Symbol	Parameter	DDR5-3200-6400	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1

Note(s):
1. V_{pk-pk} is the mean high voltage minus the mean low voltage over TBD samples.

2.5 Single-Ended Output Levels - VOL/VOH for Loopback Signals

Table 24 — Single-ended Output levels for Loopback Signals DDR5-3200 to DDR5-6400

Symbol	Parameter	DDR5-3200-6400	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1

Note(s):
1. V_{pk-pk} is the mean high voltage minus the mean low voltage over TBD samples.

2.6 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL} and V_{OH} for single ended signals as shown in Table 25 and Figure 25.

Table 25 — Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}	V_{OH}	$[V_{OH}-V_{OL}]$ / delta TRse
Single ended output slew rate for falling edge	V_{OH}	V_{OL}	$[V_{OH}-V_{OL}]$ / delta TFse

Note(s):
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

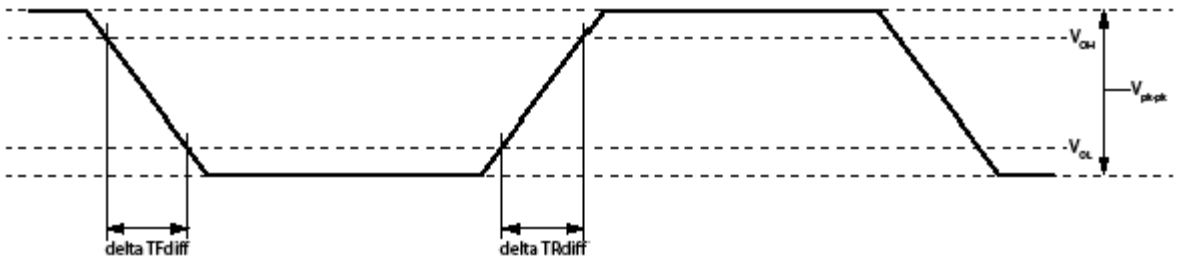


Figure 25 — Single-ended Output Slew Rate Definition

Table 26 — Single-ended Output Slew Rate for DDR5-3200 to DDR5-4800

Speed		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Single ended output slew rate	SRQse	8	18	8	18	8	18	8	18	8	18	V/ns	

Note(s):

2.7 Differential Output Levels

Table 27 — Differential Output levels for DDR5-3200 to DDR5-6400

Symbol	Parameter	DDR5-3200-6400	Units	Notes
V_{OHdiff}	Differential output high measurement level (for output SR)	0.75 x $V_{diffpk-pk}$	V	1
V_{OLdiff}	Differential output low measurement level (for output SR)	0.25 x $V_{diffpk-pk}$	V	1

Note(s):
1. $V_{diffpk-pk}$is the mean high voltage minus the mean low voltage over TBD samples.

2.8 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL-diff}$ and V_{OHdiff} for differential signals as shown in Table 28 and Figure 26

Table 28 — Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}	V_{OHdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}	V_{OLdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TFdiff

Note(s):
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

Figure 26 — Differential Output Slew Rate Definition

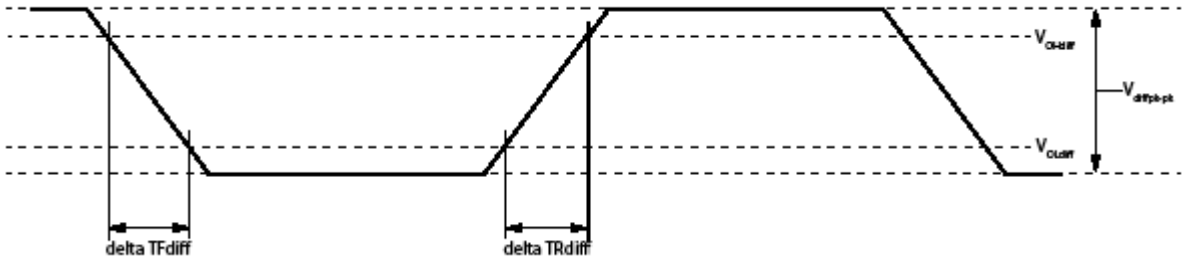


Table 29 — Differential Output Slew Rate for DDR5-3200 to DDR5-4800

Speed		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Differential output slew rate	SRQdiff	16	36	16	36	16	36	16	36	16	36	V/ns	

Note(s):

2.9 Tx DQS Jitter

Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in **Table 30**.

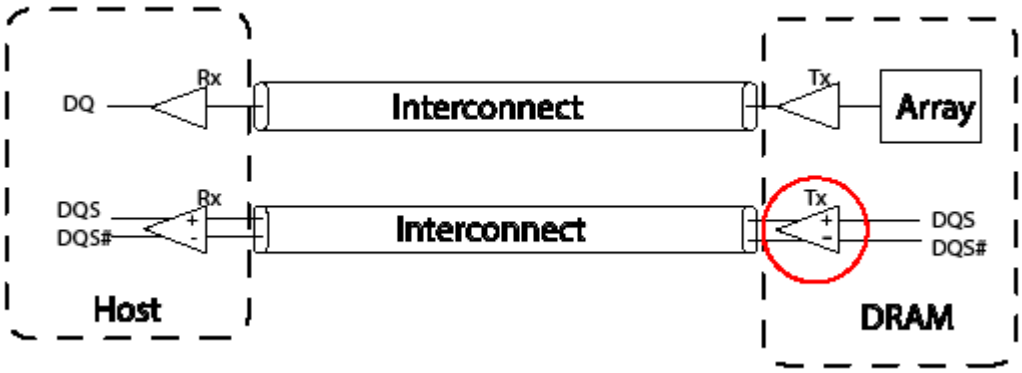


Table 30 — Tx DQS Jitter Parameters for DDR5-3200 to 4800

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rj RMS Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,4, 5,6,7,8,9, 10,11,12
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	1,2,3,5,6,7 ,8,9,10,11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 4	tTx_DQS_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,5,6,7 ,8,9,10,11, 12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 4	tTx_DQS_NUI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	1,2,3,5,6,7 ,8,9,10,11

Note(s)

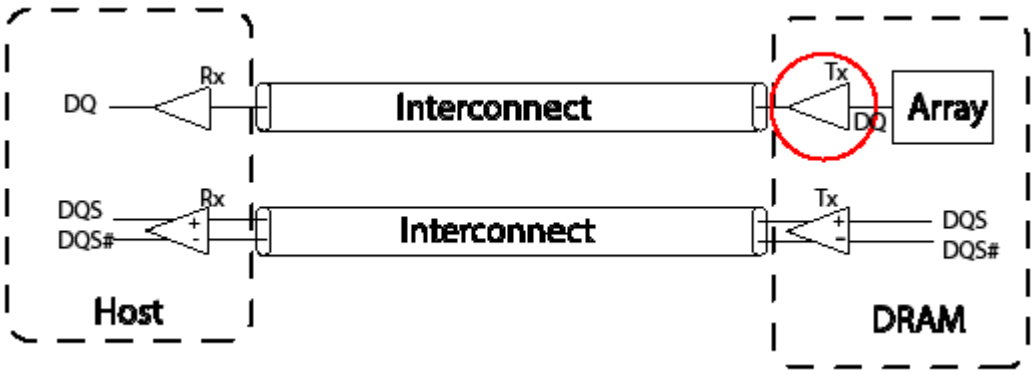
1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3. The validation methodology for these parameters will be covered in future ballots
4. Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD
5. See Section 7.2 for details on the minimum BER requirements
6. See Section 7.3 for details on UI, NUI and Jitter definitions
7. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Duty Cycle Adjuster feature prior to running the Tx DQ Jitter test
8. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44
9. Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test

10. These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.
11. Tested on the CTC2 card only
12. The max value of tTx_DQS_Rj_1UI_NoBUJ and tTx_DQS_Rj_NUI_NoBUJ can be 6mUI RMS

2.10 Tx DQ Jitter

2.10.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in **Table 31**.



2.10.2 Tx DQ Jitter Parameters

Table 31 — Tx DQ Jitter Parameters for DDR5-3200 to 4800

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rj RMS of 1-UI jitter without BUJ	tTx_DQ_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1,3,4,5,7,8,9,10,11,12,13,14
Dj pp 1-UI jitter without BUJ	tTx_DQ_1UI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	3,5,7,8,9,10,11,12,13
Rj RMS of N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj NoBUJ + 0.002	-	tCK_NUI_Rj NoBUJ + 0.002	-	tCK_NUI_Rj NoBUJ + 0.002	UI (RMS)	3,5,7,8,9,10,11,12,13,14
Dj pp N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	3,6,7,8,9,10,11,12,13
Delay of any data lane relative to strobe lane	tTx_DQS2DQ	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	UI	3,5,6,7,9,10,11,12,13

Note(s):

1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3. The validation methodology for these parameters will be covered in future ballots
4. Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD
5. Delay of any data lane relative to strobe lane, as measured at Tx output
6. Vref noise level to DQ jitter should be adjusted to minimize DCD
7. See **Chapter 7** for details on the minimum BER requirements
8. See **Chapter 7** for details on UI, NUI and Jitter definitions
9. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test
10. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.
11. Spread Spectrum Clocking (SSC) must be disabled while running this test
12. These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.
13. Tested on the CTC2 card only
14. The max value of tTx_DQ_Rj_1UI_NoBUJ and tTx_DQ_Rj_NUI_NoBUJ can be 6mUI RMS

2.11 Tx DQ Stressed Eye

Tx DQ stressed eye height and eye width must meet minimum specification values at BER=E^{-9} and confidence level 99.5%. Tx DQ Stressed Eye shows the DQS to DQ skew for both Eye Width and Eye Height. In order to support different Host Receiver (Rx) designs, it is the responsibility of the Host to insure the advanced DQS edges are adjusted accordingly via the Read DQS Offset Timing mode register settings (MR40 OP[3:0]).

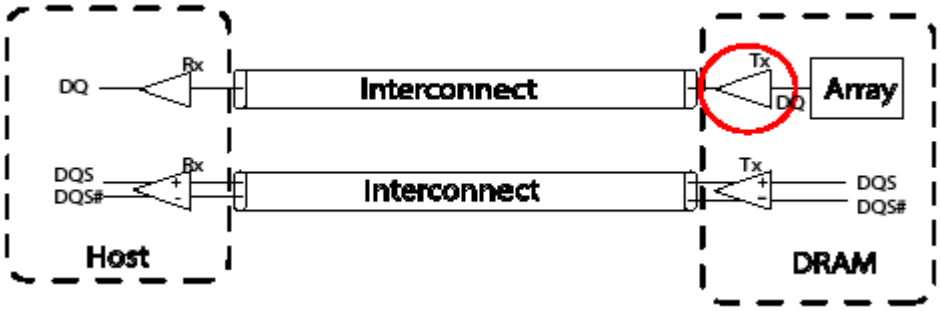


Figure 27 — Example of DDR5 Memory Interconnect

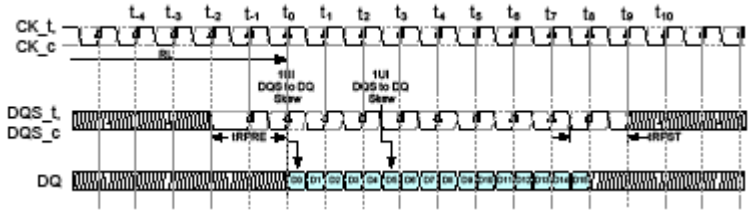


Figure 28 — Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 1 UI skew

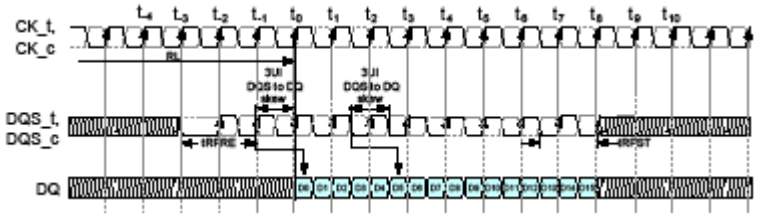


Figure 29 — Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 3 UI skew with Read DQS Offset Timing set to 1 Clock (2UI)

2.11.1 Tx DQ Stressed Eye Parameters

Table 32 — Tx DQ Stressed Eye Parameters for DDR5-3200 to 4800

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate, SES=Stressed Eye Skew]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Eye Height specified at the transmitter with a skew between DQ and DQS of 1UI	TxEH_DQ_SES_1UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 1UI	TxEW_DQ_SES_1UI	0.72	-	0.72	-	0.72	-	0.72	-	0.72	-	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 2UI	TxEH_DQ_SES_2UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 2UI	TxEW_DQ_SES_2UI	0.72	-	0.72	-	0.72	-	0.72	-	0.72	-	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 3UI	TxEH_DQ_SES_3UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 3UI	TxEW_DQ_SES_3UI	0.72	-	0.72	-	0.72	-	0.72	-	0.72	-	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 4UI	TxEH_DQ_SES_4UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	mV	1,2,3,4,5,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 4UI	TxEW_DQ_SES_4UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	UI	1,2,3,4,5,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 5UI	TxEH_DQ_SES_5UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	mV	1,2,3,4,5,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 5UI	TxEW_DQ_SES_5UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	UI	1,2,3,4,5,6,7,8,9,10

Note(s):

1. Minimum BER E^{-9} and Confidence Level of 99.5% per pin
2. Refer to the minimum Bit Error Rate (BER) requirements for DDR5
3. The validation methodology for these parameters will be covered in future ballot(s)
4. Mismatch is defined as DQS to DQ mismatch, in UI increments
5. The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable
6. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test
7. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQS are MR103-MR110, the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.
8. Spread Spectrum Clocking (SSC) must be disabled while running this test
9. These parameters are tested using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.
10. Tested on the CTC2 card only

11. Matched DQS to DQ would require the DQs to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI mismatch would require the DQS to be adjusted 1.5UI. Generally, for XUI mismatch the DQ must be adjusted XUI + 0.5UI to be placed in the center of the eye.

3. IDD, IDDQ, IPP Specification Parameters and Test conditions

3.1 IDD, IPP and IDDQ Measurement Conditions

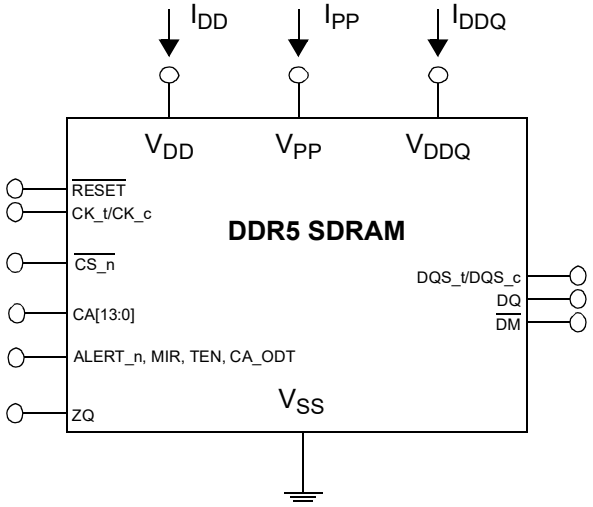
In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 30 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDDQ0, IPP0, IDD0F, IDDQ0F, IPP0F, IDD2N, IDDQ2N, IPP2N, IDD2NT, IDDQ2NT, IPP2NT, IDD2P, IDDQ2P, IPP2P, IDD3N, IDDQ3N, IPP3N, IDD3P, IDDQ3P, IPP3P, IDD4R, IDDQ4R, IPP4R, IDD4RC, IDD4W, IDDQ4W, IPP4W, IDD4WC, IDD5F, IDDQ5F, IPP5F, IDD5B, IDDQ5B, IPP5B, IDD5C, IDDQ5C, IPP5C, IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD7, IDDQ7, IPP7, IDD8, IDDQ8, IPP8 and IDD9, IDDQ9, IPP9) are measured as time-averaged currents with all VDD balls of the DDR5 SDRAM under test tied together. Any IDDQ or IPP current is not included in IDD currents.
- IDDQ currents are measured as time-averaged currents with all VDDQ balls of the DDR5 SDRAM under test tied together. Any IDD or IPP current is not included in IDDQ currents.
- IPP currents are measured as time-averaged currents with all VPP balls of the DDR5 SDRAM under test tied together. Any IDD or IDDQ current is not included in IPP currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR5 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 31.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as VIN <= VILAC(max).
- “1” and “HIGH” is defined as VIN >= VIHAC(min).
- “MID-LEVEL” is defined as inputs are VREF = 0.75 * VDDQ.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 266.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 265.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 288 through Table 288.
- IDD Measurements are done after properly initializing and training the DDR5 SDRAM. This includes but is not limited to setting
  TDQS_t disabled in MR5;
  CRC disabled in MR50;
  DM disabled in MR5;
  1N mode enabled and set CS assertion duration (MR2:OP[4]) as 1_B in MR2, unless otherwise specified in the IDD, IDDQ and IPP patterns’ conditions definitions;
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD, IDDQ or IPP measurement is started, with the exception of IDD9 which can be measured any time after the DRAM has entered MBIST mode.
  .
- T_{CASE} defined as 0 - 95°C, unless stated in the specific condition definition table below.
- For all IDD, IDDQ and IPP measurement loop timing parameters, refer to the timing parameters defined in the spec to calculate the nCK required.



Note(s):
1. DIMM level Output test load condition may be different from above

Figure 30 — Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

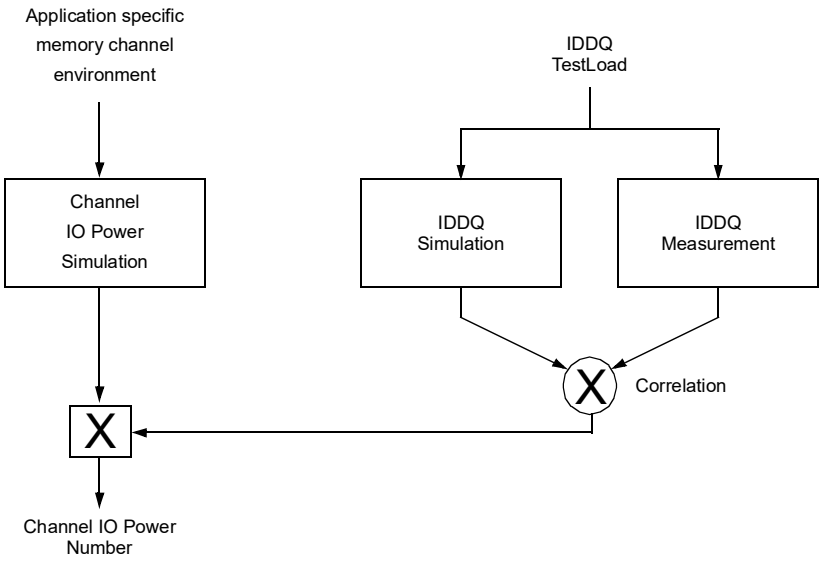


Figure 31 — Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** **External clock:** On; **tCK, nRC, nRAS, nRP, nRRD**: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to Table 288 on page 411; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 288 on page 411); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 288 on page 411
IDDQ0	**Operating One Bank Active-Precharge IDDQ Current** **Same condition with IDD0,** however measuring IDDQ current instead of IDD current
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0,** however measuring IPP current instead of IDD current
IDD0F	**Operating Four Bank Active-Precharge Current** **External clock:** On; **tCK, nRC, nRAS, nRP, nRRD**: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to Table 279 on page 418; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with four bank active at a time: (see Table 279 on page 418); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 279 on page 418
IDDQ0F	**Operating Four Bank Active-Precharge IDDQ Current** **Same condition with IDD0F,** however measuring IDDQ current instead of IDD current
IPP0F	**Operating Four Bank Active-Precharge IPP Current** **Same condition with IDD0F,** however measuring IPP current instead of IDD current
IDD2N	**Precharge Standby Current** **External clock:** On; **tCK**: see Table 266 on page 404; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to Table 280 on page 425; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 280 on page 425
IDDQ2N	**Precharge Standby IDDQ Current** **Same condition with IDD2N,** however measuring IDDQ current instead of IDD current
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N,** however measuring IPP current instead of IDD current
IDD2NT	**Precharge Standby Non-Target Command Current** **External clock:** On; **tCK**: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** High between WRITE commands; **CS_n, CA Inputs:** partially toggling according to Table 281 on page 426; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 281 on page 426
IDDQ2NT (Optional)	**Precharge Standby Non-Target Command IDDQ Current** Same condition with IDD2NT, however measuring IDDQ current instead of IDD current
IPP2NT (Optional)	**Precharge Standby Non-Target Command IPP Current** Same condition with IDD2NT, however measuring IPP current instead of IDD current

Symbol	Description
IDD2P	**Precharge Power-Down** **Device in Precharge Power-Down, External clock:** On; **tCK**: see Table 266 on page 404; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IDDQ current instead of IDD current
IPP2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IPP current instead of IDD current
IDD3N	**Active Standby Current** **External clock:** On; **tCK**: see Table 266 on page 404; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to Table 280 on page 425; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 280 on page 425
IDDQ3N	**Active Standby IDDQ Current** **Same condition with IDD3N,** however measuring IDDQ current instead of IDD current
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N,** however measuring IPP current instead of IDD current
IDD3P	**Active Power-Down Current** **Device in Active Power-Down, External clock:** On; **tCK**: see Table 266 on page 404; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ3P	**Active Power-Down IDDQ Current** **Same condition with IDD3P,** however measuring IDDQ current instead of IDD current
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P,** however measuring IPP current instead of IDD current
IDD4R	**Operating Burst Read Current** **External clock:** On; **tCK, nCCD, CL**: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** High between RD; **CA Inputs:** partially toggling according to Table 282 on page 427; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 282 on page 427; **DM_n:** stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 282 on page 427); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 282 on page 427
IDD4RC	**Operating Burst Read Current with Read CRC** **Read CRC enabled[4]. Other conditions:** see IDD4R
IDDQ4R	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R,** however measuring IPP current instead of IDD current
IDD4W	**Operating Burst Write Current** **External clock:** On; **tCK, nCCD, CL**: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** High between WR; **CA Inputs:** partially toggling according to Table 283 on page 432; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 283 on page 432; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 283 on page 432); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 283 on page 432
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3], Other conditions:** see IDD4W
IDDQ4W	**Operating Burst Write IDDQ Current** **Same condition with IDD4W,** however measuring IDDQ current instead of IDD current
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W,** however measuring IPP current instead of IDD current
IDD5B	**Burst Refresh Current (Normal Refresh Mode)** **External clock:** On; **tCK, nRFC**1: see Table 266 on page 404; **BL:** 16[1]; **CS_n**: High between REF; **CA Inputs:** partially toggling according to Table 285 on page 441; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC1 (see Table 285 on page 441); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 285 on page 441
IDDQ5B	**Burst Refresh IDDQ Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IDDQ current instead of IDD current
IPP5B	**Burst Refresh IPP Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IPP current instead of IDD current
IDD5F	**Burst Refresh Current (Fine Granularity Refresh Mode)** **tRFC=tRFC2, Other conditions:** see IDD5B
IDDQ5F	**Burst Refresh IDDQPP Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IDDQ current instead of IDD current

Symbol	Description
IPP5F	**Burst Refresh IPP Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IPP current instead of IDD current
IDD5C	**Burst Refresh Current (Same Bank Refresh Mode)** **External clock:** On; **tCK, nRFCsb**: see Table 189 on page 404; **BL:** 16[1]; **CS_n**: High between REF; **CA Inputs:** partially toggling according to Table 286 on page 446; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFCsb (see Table 286 on page 446); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 286 on page 446
IDDQ5C	**Burst Refresh IDDQPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IDDQ current instead of IDD current
IPP5C	**Burst Refresh IPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IPP current instead of IDD current
IDD6N	**Self Refresh Current: Normal Temperature Range** ***T*CASE:** 0 - 85°C; **External clock:** Off; CK_t and CK_c#: HIGH; tCK, nCPDED: see Table 266 on page 404; **BL:** 16[1]; **CS_n#:** low; **CA, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** All ODT disabled in MR32-MR35;
IDDQ6N	**Self Refresh IDDQ Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IDDQ current instead of IDD current
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IPP current instead of IDD current
IDD6E	**SelfRefresh Current: Extended Temperature Range**) ***T*CASE:** 85 - 95°C; Extended[4]; **External clock:** Off; CK_t and CK_c: HIGH; tCK, nCPDED: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** low; **CA, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]
IDDQ6E	**Self Refresh IDDQ Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IDDQ current instead of IDD current
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IPP current instead of IDD current
IDD7	**Operating Bank Interleave Read Current** **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD_S, nFAW, tCCD_S CL**: see Table 266 on page 404; **BL:** 16[1]; **CS_n**: High between ACT and RDA; **CA Inputs:** partially toggling according to Table 288 on page 444; **Data IO:** read data bursts with different data between one burst and the next one according to Table 288 on page 444; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 288 on page 444; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 288 on page 444
IDDQ7	**Operating Bank Interleave Read IDDQ Current** **Same condition with IDD7,** however measuring IDDQ current instead of IDD current
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7,** however measuring IPP current instead of IDD current
IDD8	**Maximum Power Saving Deep Power Down Current** **External clock:** Off; CK_t and CK_c#: HIGH; tCK, nCPDED: see Table 266 on page 404; **BL:** 16[1]; **CS_n#:** low; **CA:**High**, DM_n:** stable at 1; **Bank Activity:** All banks closed and device in MPSM deep power down mode5; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Patterns Details**: same as IDD6N but MPSM is enabled in mode register.
IDDQ8	**Maximum Power Saving Deep Power Down IDDQ Current** **Same condition with IDD8,** however measuring IDDQ current instead of IDD current
IPP8	**Maximum Power Saving Deep Power Down IPP Current** **Same condition with IDD8,** however measuring IPP current instead of IDD current
IDD9 (Optional)	**MBIST Current** **Device in MBIST mode, External clock:** On; **CS_n**: Stable at 1 after MBIST entry; **CA Inputs:** stable at 1; **Data IO:** VDDQ; **Bank Activity:** MBIST operation; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ9 (Optional)	**MBIST IDDQ Current** **Same condition with IDD9,** however measuring IDDQ current instead of IDD current
IPP9 (Optional)	**MBIST IPP Current** **Same condition with IDD9,** however measuring IPP current instead of IDD current

Note(s):

1. Burst Length: BL16 fixed by MR0 OP[1:0]=00.

2. Output Buffer Enable
   - set MR5 OP[0] = 0] : Qoff = Output buffer enabled
   - set MR5 OP[2:1] = 00]: Pull-Up Output Driver Impedance Control = RZQ/7
   - set MR5 OP[7:6] = 00]: Pull-Down Output Driver Impedance Control = RZQ/7

   RTT_Nom enable

- set MR35 OP[5:0] = 110110: RTT_NOM_WR = RTT_NOM_RD = RZQ/6
RTT_WR enable
- set MR34 OP[5:3] = 010 RTT_WR = RZQ/2
CA/CS/CK ODT, DQS_RTT_PART, and RTT_PARK disable
- set MR32 OP[5:0] = 000000
- set/MR33 OP[5:0] = 000000

- set MR34 OP[2:0] = 000

3. WRITE CRC enabled
- set MR50 OP[2:1] = 11

4. Read CRC enabled
- set MR50:OP[0]=1

5. MPSM Deep Power Down Mode
- set MR2:OP[3]=1 if PDA Enumerate ID not equal to 15
- set MR2:OP[5]=1 if PDA Enumerate ID equal to 15

11.2 IDD0, IDDQ0, IPP0 Pattern

Executes Active and PreCharge commands with tightest timing possible while exercising all Bank and Bank Group addresses. Note 2 applies to the entire table.

Table 33 — IDD0, IDDQ0, IPP0

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H	-	0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling1					Repeat sequence to satisfy tRAS(min), truncate if required
	2	PREpb	L	-		0x0	0x00	0x0	
	3	DES	H	Toggling1					Repeat sequence to satisfy tRP(min), truncate if required
	4	ACT	L H	-	0x03FFF	0x0	0x00	0x0	
	5	DES	H	Toggling1					Repeat sequence to satisfy tRAS(min), truncate if required
	6	PREpb	L	-		0x0	0x00	0x0	
	7	DES	H	Toggling1					Repeat sequence to satisfy tRP(min), truncate if required
1	8-15	Repeat sub-loop 0, use BG[2:0]=0x1 instead							
2	16-23	Repeat sub-loop 0, use BG[2:0]=0x2 instead							
3	24-31	Repeat sub-loop 0, use BG[2:0]=0x3 instead							
4	32-39	Repeat sub-loop 0, use BG[2:0]=0x4 instead							skip for x16
5	40-47	Repeat sub-loop 0, use BG[2:0]=0x5 instead							skip for x16
6	48-55	Repeat sub-loop 0, use BG[2:0]=0x6 instead							skip for x16
7	56-63	Repeat sub-loop 0, use BG[2:0]=0x7 instead							skip for x16
8-15	64-127	Repeat sub loops 0-7, use BA[1:0]=0x1 instead							
16-23	128-191	Repeat sub loops 0-7, use BA[1:0]=0x2 instead							
24-31	192-255	Repeat sub loops 0-7, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-31 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

Note(s):

1. Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For 3DS, all banks of all “non-target” logical ranks are Idd2N condition.

11.3 IDD0F, IDDQ0F, IPP0F Pattern

Executes a rolling four bank group Active and PreCharge commands per tRC time while exercising all Bank, Bank, Group and CID addresses. Note 2 applies to the entire table.

Table 34 — IDD0F, IDDQ0F, IPP0F

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H		0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	2	ACT	L H		0x00000	0x0	0x01	0x0	
	3	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	4	ACT	L H		0x00000	0x0	0x02	0x0	
	5	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	6	ACT	L H		0x00000	0x0	0x03	0x0	
	7	DES	H	Toggling1					Repeat to satisfy tRAS(min) from Sequence 0
	8	PREpb	L			0x0	0x00	0x0	
	9	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	10	PREpb	L			0x0	0x01	0x0	
	11	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	12	PREpb	L			0x0	0x02	0x0	
	13	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	14	PREpb	L			0x0	0x03	0x0	
	15	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	16	DES	H	Toggling1					Repeat for tRC(min) from Sequence 0 first ACTIVATE. This will be zero DESELECTS for speed 4000Mbps and slower.
1	17-33	Repeat sub-loop 0, use Row Address = 0x03FFF for the ACT instead							
2-3	34-67	Repeat sub-loop 0-1, use BG[2:0]=0x4,0x5,0x6,0x7 instead of 0x0,0x1,0x2,0x3							skip for x16
4-7	68-101	Repeat sub-loops 0-3, use BA[1:0]=0x1 instead							
8-11	102-135	Repeat sub-loops 0-3, use BA[1:0]=0x2 instead							
12-15	136-169	Repeat sub-loops 0-3, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-15 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

Note(s):

1. Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For 3DS, all banks of all “non-target” logical ranks are Idd2N condition.

11.4 IDD2N, IDD3N Pattern

Executes DESELECT commands while exercising all command/address pins in a predefined pattern. All notes apply to entire table.

Table 35 — IDD2N, IDDQ2N, IPP2N, IDD3N, IDDQ3N, IPP3N

Sequence	Command	CS	C/A [13:0]
0	DES	H	0x0000
1	DES	H	0x3FFF
2	DES	H	0x3FFF
3	DES	H	0x3FFF

Note(s):
1. Data is pulled to VDDQ
2. DQS_t and DQS_c are pulled to VDDQ
3. Command / Address ODT is disabled
4. Repeat sequence 0 through 3.
5. All banks of all logical ranks mimic the same test condition.

11.5 IDD2NT, IDDQ2NT, IPP2NT Pattern

Executes Non-Target WRITE commands simulating Rank to Rank timing while exercising all C/A bits. Notes 3-6 apply to entire table.

Table 36 — IDD2NT, IDDQ2NT, IPP2NT

Sequence	Command	CS_n	C/A [13:0]	Special Instructions
0	WRITE1	L	0x002D	All valid C/A inputs to VSS
		L	0x0000	
1	DES	H	Toggling2	Repeat sequence to meet 1*tCCD_S(min), truncate if required
2	WRITE1	L	0x3FED	All valid C/A inputs to VDDQ
		L	0x3FFF	
3	DES	H	Toggling2	Repeat sequence to meet 1*tCCD(min), truncate if required

Note(s):
1. WRITE with CS_n=L on both cycles indicated a non-target WRITE.
2. Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
3. Time between Non-Target WRITEs reflect tCCD_S (min) for ~~two~~ one rank~~s~~.
4. DQ signals are VDDQ.
5. DQS_t, DQS_c are VDDQ.
6. Repeat 0 through 3.

11.6 IDD4R, IDDQ4R, IPP4R Pattern

Executes READ commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses.
Notes 2-9 apply to entire table

Table 37 — IDD4R, IDDQ4R, IPP4R

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	READ	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	READ	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	READ	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	READ	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. READs performed with Auto Precharge = H, Burst Chop = H.
3. Row address is set to 0x0000
4. Data reflects burst length of 16.
5. Data Pattern A for x4: 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0x0, 0xF.
6. Data Pattern B for x4: 0xF, 0x0, 0x0, 0xF, 0x~~0~~F, 0x0, 0xF, 0x~~F~~0, 0x~~F~~0, 0xF, 0x~~0~~F, 0x0, 0xF, 0x0, 0xF, 0x0.
7 Data Pattern for x8 each beat will reflect two like nibbles (Data Pattern A = 0x00, 0xFF, 0xFF...).
8. Data Pattern for x16 each beat will reflect two like bytes (Data Pattern A = 0x0000, 0xFFFF, 0xFFFF...).
9. Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state

11.7 IDD4W, IDDQ4W, IPP4W Pattern

Executes WRITE commands with tightest timing possible while exercising all Bank, Bank Group and ~~CDI~~ CID addresses. Notes 2-6 apply to entire table.

Table 38 — IDD4W, IDDQ4W, IPP4W

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	WRITE	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	WRITE	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	WRITE	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	WRITE	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands ~~as specified~~ per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. WRITEs performed with Auto Precharge = H, Burst Chop = H.
3. Row address is set to 0x0000.
4. Data reflects burst length of 16.
5. Refer to IDD4R measurement loop table for data pattern definition.
6. Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state.

11.8 IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F Pattern

Executes Refresh (all Banks) command at minimum tRFC. Notes 3-6 apply to entire table.

Table 39 — IDD5B, IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F

Sequence	Command	CS	C/A [13:0]	CA[9:8]	CID [2:0]	Special Instructions
0	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
1	DES	H	Toggling1	-	-	Repeat sequence to satisfy tRFC(min)2, truncate if required
2	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
3	DES	H	Toggling1	-	-	Repeat sequence to satisfy tRFC(min)2, truncate if required
...	Repeat sequence 0-3 for each 3DS logical rank, if applicable					CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For IDD5B, use tRFC1(min). For IDD5F, use tRFC2(min).
3. DQ signals are VDDQ.
4. All banks of all “non-target” logical ranks are Idd2N condition.
5. Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.
6. Must set CA8=H on REFab commands to indicate 1X refresh rate on devices that support RIR.

11.9 IDD5C, IDDQ5C and IPP5C Patterns

Executes Refresh (Same Bank) command at minimum tRFCsb. Notes 2-5 apply to entire table.

Table 40 — IDD5C, IDDQ5C, IPP5C

Sequence	Command	CS	C/A [13:0]	CA[9:8]	BA [1:0]	CID [2:0]	Special Instructions
0	REFsb	L	-	H	0x0	0x0	
1	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
2	REFsb	L	-	H	0x1	0x0	
3	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
4	REFsb	L	-	H	0x2	0x0	
5	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
6	REFsb	L	-	H	0x3	0x0	
7	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
...	Repeat sequence 0-7 for each 3DS logical rank, if applicable						CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. DQ signals are VDDQ.
3. All banks of all “non-target” logical ranks are Idd2N condition.
4. Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.
5. All banks of all “non-target” logical ranks are Idd2N condition.

11.10 IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R Pattern

All notes apply to entire table.

Table 41 — IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E

Sequence	Command	Clock	CS	C/A [13:0]	Special Instructions
0	SRE	Valid	L	0x3BF7	Clocks must be valid tCKLCS(min) time
1	DES	Valid	H	0x3FFF	Repeat sequence to satisfy tCPDED(min), truncate if required
2	All C/A=H	Valid	L	0x3FFF	
3	All C/A = H	CK_t = CK_c = H	L	0x3FFF	Repeat sequence indefinitely

Note(s):
1. Data is pulled to VDDQ
2. DQS_t and DQS_c are pulled to VDDQ
3. For 3DS, all banks of all logical ranks mimic the same test condition.

11.11 IDD7, IDDQ7 and IPP7 Patterns

Executes ACTVATE, READ/A commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-6 apply to entire table.

Table 42 — IDD7, IDD7Q, IPP7

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	ACT	L H	-	0x00000	-	0x0	0x0	0x0	-	
	1	DES	H	Toggling1							Repeat sequence to satisfy tRRD_S(min)
1	2	ACT	L H	-	0x03FFF	-	0x0	0x1	0x0	-	
	3	DES	H	Toggling1							Repeat sequence to satisfy tRRD_S(min)
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead									
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead									
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead									skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead									skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead									skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead									skip for x16
8	16	RDA	L H	-	-	0x3F0	0x0	0x0	0x0	Pattern A	
	17	ACT	L H	-	0x00000	-	0x1	0x0	0x0	-	
	18	DES	H	Toggling1							Repeat sequence to satisfy tCCD_S(min)
9	19	RDA	L H	-	-	0x000	0x0	0x1	0x0	Pattern B	
	20	ACT	L H	-	0x03FFF	-	0x1	0x1	0x0	-	
	21	DES	H	Toggling1							Repeat sequence to satisfy tCCD_S(min)
10	22-24	Repeat sub-loop 8, use BG[2:0]=0x2 instead									
11	25-27	Repeat sub-loop 9, use BG[2:0]=0x3 instead									
12	28-30	Repeat sub-loop 8, use BG[2:0]=0x4 instead									skip for x16
13	31-33	Repeat sub-loop 9, use BG[2:0]=0x5 instead									skip for x16
14	34-36	Repeat sub-loop 8, use BG[2:0]=0x6 instead									skip for x16
15	37-39	Repeat sub-loop 9, use BG[2:0]=0x7 instead									skip for x16
16-23	40-64	Repeat sub-loops 8-15, use BA[1:0]=0x1 for the RDA and BA[1:0]=0x2 for the ACT									
24-31	65-89	Repeat sub-loops 8-15, use BA[1:0]=0x2 for the RDA and BA[1:0]=0x3 for the ACT									
32-39	90-114	Repeat sub-loops 8-15, use BA[1:0]=0x3 for the RDA and BA[1:0]=0x0 for the ACT									
...	...	Repeat sub-loops 0-18 for each 3DS logical rank, if applicable									CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. READs performed with Auto Precharge = L, Burst Chop = H.
3. x8 or x16 may have different Bank or Bank Group Address.
4. Data reflects burst length of 16.
5. Refer to IDD4R measurement loop table for data pattern definition
6. For 3DS, all banks of all “non-target” logical ranks are Idd2N condition

Standard Speed Bins

DDR5-4400 Speed Bins and Operations

Speed Bin				Symbol	DDR5-4400B		Unit	NOTE
CL-nRCD-nRP					36-36-36			
Parameter					min	max		
Internal read command to first data				tAA	16.000		ns	
ACT to internal read or write delay time				tRCD	16.000		ns	7
Row Precharge Time				tRP	16.000		ns	7
ACT to PRE command period				tRAS	32.00	5 x tREFI1	ns	7
ACT to ACT or REF command period				tRC	48.000		ns	7,8
CAS Write Latency				CWL	CWL=CL-2 (34)		ns	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL Write CWL	Supported Frequency Down Bins				
	20.952	-	CL=22, CWL=20	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	CL=28, CWL=26	tCK(AVG)	0.625	0.681	ns	
3200BN 3200B	16.250	16.250	CL=26, CWL=24	tCK(AVG)	0.625	0.681	ns	
3200AN	15.000	15.000	CL=24, CWL=22	tCK(AVG)	RESERVED		ns	
3600C	17.777	17.777	CL=32, CWL=30	tCK(AVG)	0.555	<0.625	ns	
3600BN 3600B	16.666	16.666	CL=30, CWL=28	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	CL=26, CWL=24	tCK(AVG)	RESERVED		ns	
4000C	18.000	17.500	CL=36, CWL=34	tCK(AVG)	0.500	<0.555	ns	
4000BN 4000B	16.000	16.000	CL=32, CWL=30	tCK(AVG)	0.500	<0.555	ns	
4000AN	14.000	14.000	CL=28, CWL=26	tCK(AVG)	RESERVED		ns	
4400C	18.181	17.727	CL=40, CWL=38	tCK(AVG)	0.454	<0.500	ns	
4400BN 4400B	16.363	16.363	CL=36, CWL=34	tCK(AVG)	0.454	<0.500	ns	
4400AN	14.545	14.545	CL=32, CWL=30	tCK(AVG)	RESERVED		ns	
Supported CL					22,26,28,30,32,36,40		nCK	

DDR5-4800 Speed Bins and Operations

Speed Bin				Symbol	DDR5-4800B		Unit	NOTE
CL-nRCD-nRP					40-39-39			
Parameter					min	max		
Internal read command to first data				tAA	16.000		ns	
ACT to internal read or write delay time				tRCD	16.000		ns	7
Row Precharge Time				tRP	16.000		ns	7
ACT to PRE command period				tRAS	32.00	5 x tREFI1	ns	7
ACT to ACT or REF command period				tRC	48.000		ns	7,8
CAS Write Latency				CWL	CWL=CL-2 (38)		ns	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL Write CWL	Supported Frequency Down Bins				
	20.952	-	CL=22, CWL=20	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	CL=28, CWL=26	tCK(AVG)	0.625	0.681	ns	
3200BN 3200B	16.250	16.250	CL=26, CWL=24	tCK(AVG)	0.625	0.681	ns	
3200AN	15.000	15.000	CL=24, CWL=22	tCK(AVG)	RESERVED		ns	
3600C	17.777	17.777	CL=32, CWL=30	tCK(AVG)	0.555	<0.625	ns	
3600BN 3600B	16.666	16.666	CL=30, CWL=28	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	CL=26, CWL=24	tCK(AVG)	RESERVED		ns	
4000C	18.000	17.500	CL=36, CWL=34	tCK(AVG)	0.500	<0.555	ns	
4000BN 4000B	16.000	16.000	CL=32, CWL=30	tCK(AVG)	0.500	<0.555	ns	
4000AN	14.000	14.000	CL=28, CWL=26	tCK(AVG)	RESERVED		ns	
4400C	18.181	17.727	CL=40, CWL=38	tCK(AVG)	0.454	<0.500	ns	
4400BN 4400B	16.363	16.363	CL=36, CWL=34	tCK(AVG)	0.454	<0.500	ns	
4400AN	14.545	14.545	CL=32, CWL=30	tCK(AVG)	RESERVED		ns	
4800C	17.500	17.500	CL=42, CWL=40	tCK(AVG)	0.416	<0.454	ns	
4800BN	16.666	16.666	CL=40, CWL=38	tCK(AVG)	0.416	<0.454	ns	
4800B	16.666	16.250	CL=40, CWL=38	tCK(AVG)	0.416	<0.454	ns	
4800AN	14.166	14.166	CL=34, CWL=32	tCK(AVG)	RESERVED		ns	
Supported CL					22,26,28,30,32,36,40,42		nCK	

IDD Specifications

8GB, 1Gx64 Module (1Rank of x16) NECC UDIMM

IDD		unit	note
Symbol	4800		
IDD0	107.1	mA	
IDD0F	176.9	mA	
IDD2N	75.1	mA	
IDD2P	60.6	mA	
IDD3N	110.9	mA	
IDD3P	96.6	mA	
IDD4R	581.1	mA	
IDD4W	663.2	mA	
IDD5	257.6	mA	
IDD5B	245.2	mA	
IDD5C	130.5	mA	
IDD6N	63.8	mA	
IDD7	594.0	mA	
IDD8	29.2	mA	

Note(s):
Module IDD is based on PMIC 5V input current, each IDD parameter includes all IDD/IDDQ/IPP of DRAM, RCD current and PMIC efficiency.

16GB, 2Gx64 Module (1Rank of x8) NECC UDIMM

IDD		unit	note
Symbol	4800		
IDD0	169.8	mA	
IDD0F	237.9	mA	
IDD2N	137.6	mA	
IDD2P	108.7	mA	
IDD3N	209.1	mA	
IDD3P	180.5	mA	
IDD4R	693.3	mA	
IDD4W	820.2	mA	
IDD5	502.6	mA	
IDD5B	477.8	mA	
IDD5C	248.4	mA	
IDD6N	126.1	mA	
IDD7	803.2	mA	
IDD8	57.0	mA	

Note(s):

Module IDD is based on PMIC 5V input current, each IDD parameter includes all IDD/IDDQ/IPP of DRAM, RCD current and PMIC efficiency.

32GB, 4Gx64 Module (2Rank of x8) NECC UDIMM

IDD		unit	note
Symbol	4800		
IDD0	305.7	mA	
IDD0F	373.8	mA	
IDD2N	273.5	mA	
IDD2P	244.7	mA	
IDD3N	345.0	mA	
IDD3P	316.4	mA	
IDD4R	860.8	mA	
IDD4W	957.6	mA	
IDD5	638.5	mA	
IDD5B	613.7	mA	
IDD5C	384.3	mA	
IDD6N	250.5	mA	
IDD7	970.7	mA	
IDD8	112.3	mA	

Note(s):
Module IDD is based on PMIC 5V input current, each IDD parameter includes all IDD/IDDQ/IPP of DRAM, RCD current and PMIC efficiency.

16GB, 2Gx72 Module (1Rank of x8) ECC UDIMM

IDD		unit	note
Symbol	4800		
IDD0	209.2	mA	
IDD0F	294.3	mA	
IDD2N	169.0	mA	
IDD2P	133.0	mA	
IDD3N	258.4	mA	
IDD3P	222.7	mA	
IDD4R	860.9	mA	
IDD4W	1019.5	mA	
IDD5	625.2	mA	
IDD5B	594.2	mA	
IDD5C	307.5	mA	
IDD6N	157.4	mA	
IDD7	998.3	mA	
IDD8	71.0	mA	

Note(s):

Module IDD is based on PMIC 5V input current, each IDD parameter includes all IDD/IDDQ/IPP of DRAM, RCD current and PMIC efficiency.

32GB, 4Gx72 Module (2Rank of x8) ECC UDIMM

IDD		unit	note
Symbol	4800		
IDD0	376.4	mA	
IDD0F	461.5	mA	
IDD2N	336.2	mA	
IDD2P	300.2	mA	
IDD3N	425.5	mA	
IDD3P	389.8	mA	
IDD4R	1065.9	mA	
IDD4W	1187.0	mA	
IDD5	792.4	mA	
IDD5B	761.3	mA	
IDD5C	474.7	mA	
IDD6N	312.9	mA	
IDD7	1203.3	mA	
IDD8	140.1	mA	

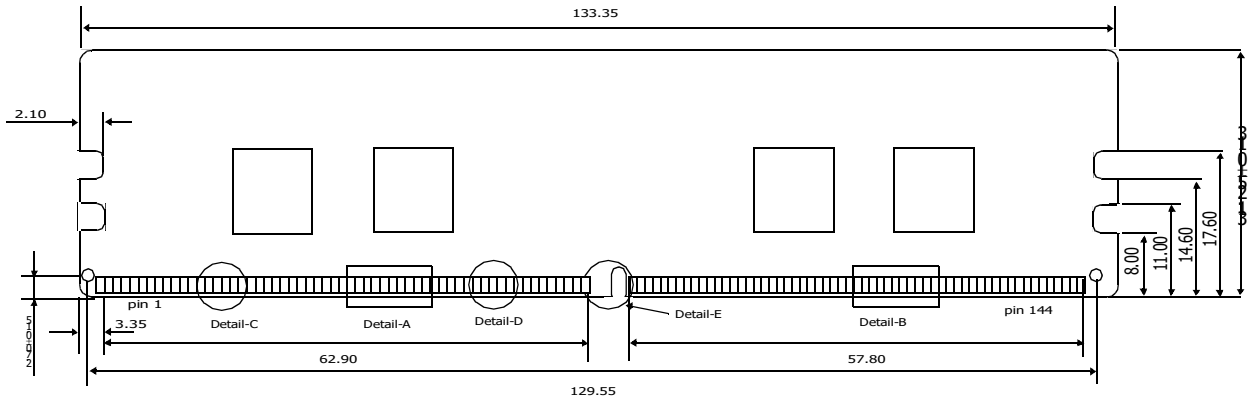
Note(s):

Module IDD is based on PMIC 5V input current, each IDD parameter includes all IDD/IDDQ/IPP of DRAM, RCD current and PMIC efficiency.

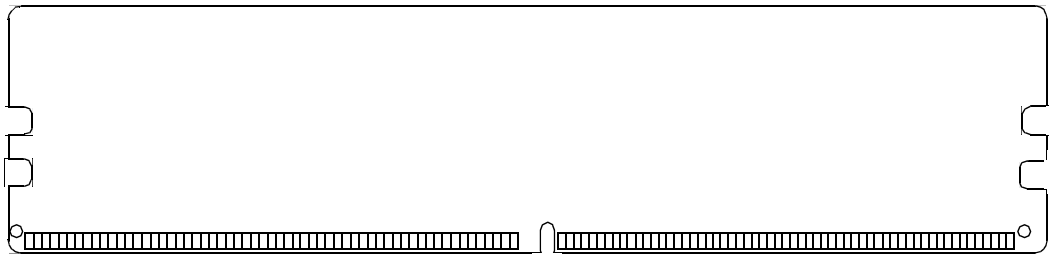
Module Dimensions

8GB 1Gx64 Module (1Rank of x16) NECC U-DIMM

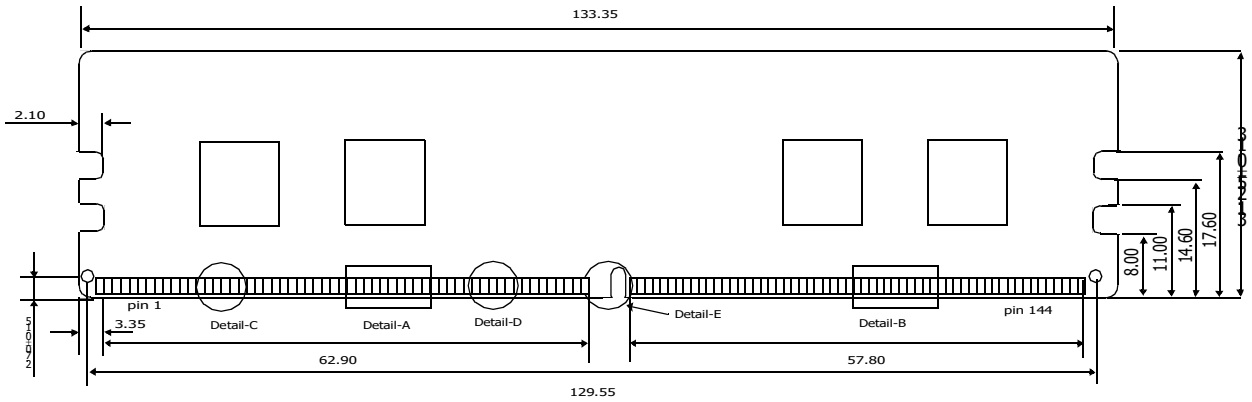
Front



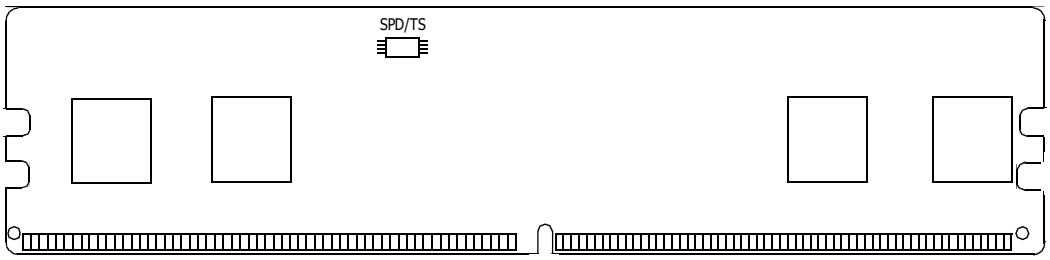
Back



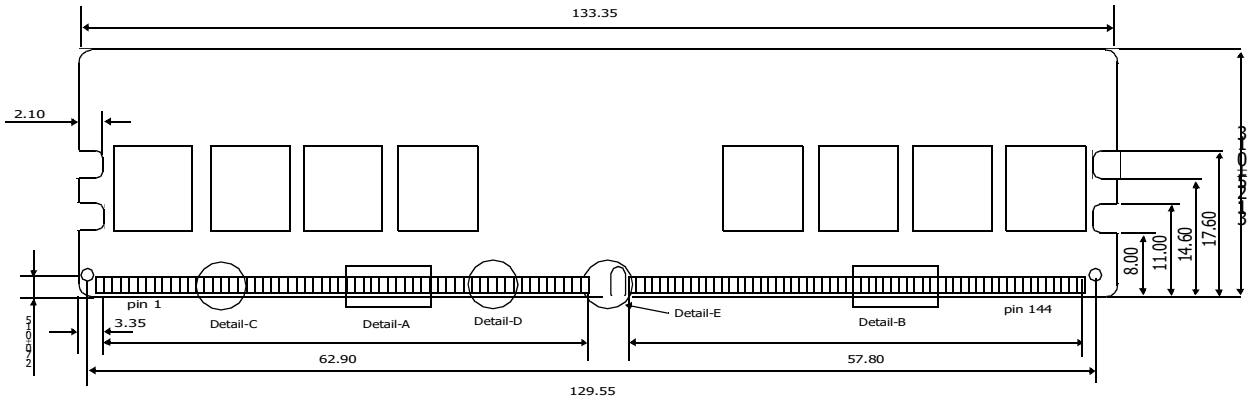
Front


133.35
2.10
31.50
17.60
14.60
11.00
8.00
5.10
4.00
2.50
pin 1
3.35
Detail-C
Detail-A
Detail-D
Detail-E
Detail-B
pin 144
62.90
57.80
129.55

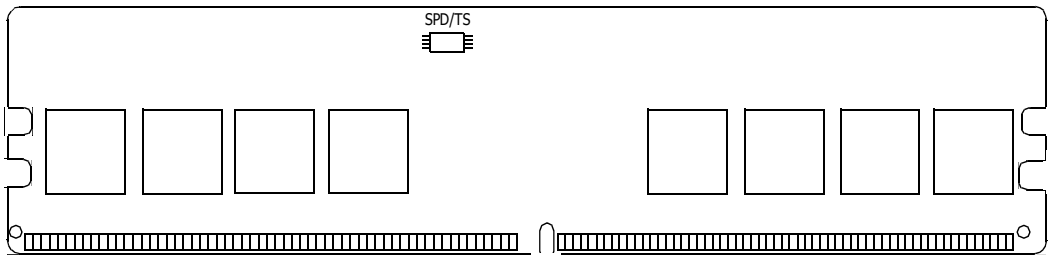
Back


SPD/TS

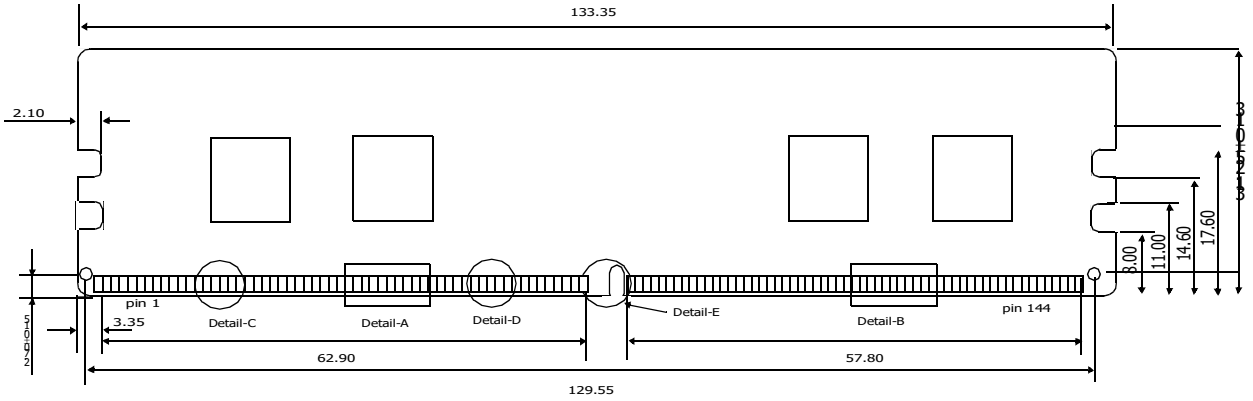
Front


133.35
2.10
30.00 Max
17.60
14.60
11.00
8.00
pin 1
3.35
Detail-C
Detail-A
Detail-D
Detail-E
Detail-B
pin 144
5.92
62.90
57.80
129.55

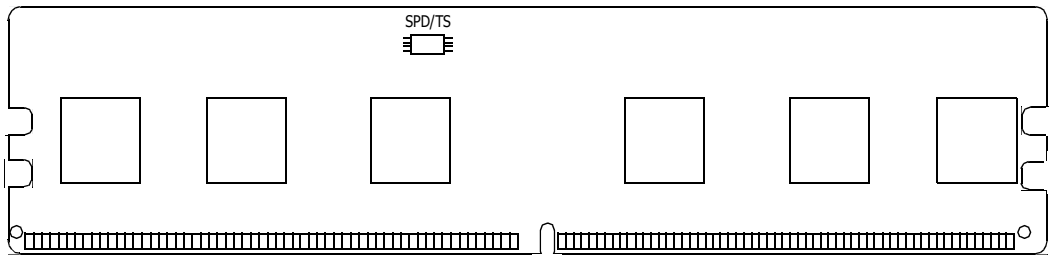
Back


SPD/TS

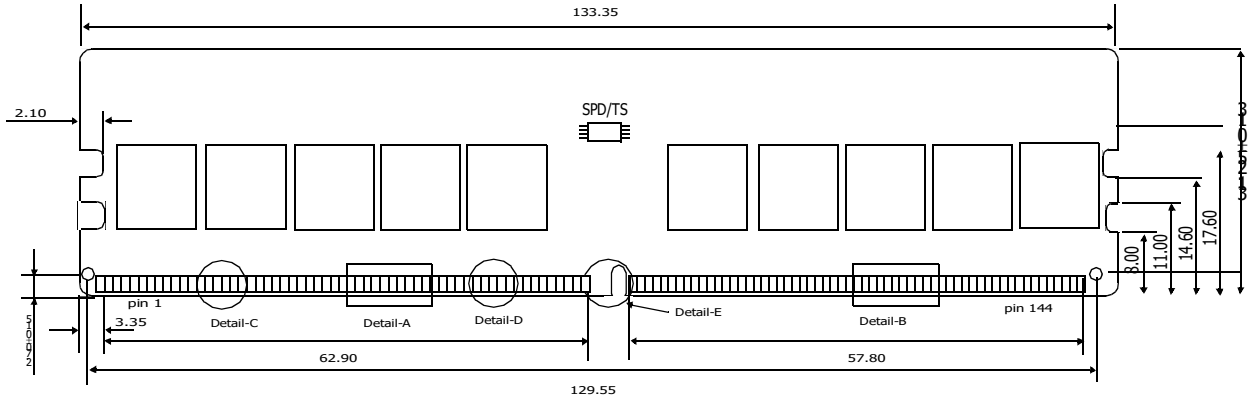
Front


133.35
2.10
pin 1
3.35
Detail-C
Detail-A
Detail-D
Detail-E
Detail-B
pin 144
62.90
57.80
129.55
3.00
11.00
14.60
17.60

Back


SPD/TS

Front


133.35
2.10
SPD/TS
8.00
11.00
14.60
17.60
pin 1
3.35
Detail-C
Detail-A
Detail-D
Detail-E
Detail-B
pin 144
62.90
57.80
129.55

Back